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DATE: December 19, 2007

PTO IDENTIFIER: Application Number 09/588,351-Conf. #8116
Patent Number

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Roy C. (deceased), Flaker et al.

Application No.: 09/588,351 Confirmation No.: 8116

Filed: June 7, 2000 Art Unit: 2815

For: CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES Examiner: J. A. Fenty

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IEEE ELECTRON DEVICE LETTERS, VOL. 14, NO. 4, APRIL 1993

Anomalous Voltage Overshoot During Turn-Off of Thin-Film n-Channel SOI MOSFET's

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Abstract—**This paper reports an anomalous output voltage overshoot observed during the turn-off of single short-channel thin-film silicon-on-insulator (SOI) n-MOSFET's. The parasitic floating-base bipolar device, triggered by impact ionization, is shown to be responsible for this effect. Because switching occurs over a subnanosecond time scale, the charge dynamics related to the bipolar action are essential to explain this voltage overshoot.**

I. Introduction

THIN-film fully depleted SOI technologies have recently demonstrated very attractive features over their bulk silicon counterparts, e.g., significant speed advantage, nearly ideal subthreshold slope, latch-up-free structures, and suppression of the kink effect [1]. On the other hand, the associated parasitic bipolar effect may still be important. For example, it can be responsible for premature breakdown and single device off-state latch-up. Other possible implications of the bipolar action have been discussed extensively by Choi and Fossum [2], [3], but mainly from a static point of view. As far as we know, no model of the parasitic bipolar charge dynamics has been considered. This paper describes a voltage overshoot observed during turn-off of a single short-channel thin-film SOI n-MOSFET. This effect is related to impact ionization, which causes a large bipolar action. Because switching occurs over a subnanosecond time scale, the charge dynamics of the parasitic bipolar transistor are essential for accurate modeling of the transient output response.

II. Experiments

The measured SOI devices were fabricated on a SIMOX wafer using a 0.25-μm CMOS technology. The top gate oxide thickness is 7 nm and the buried oxide layer thickness is 250 nm. The 50-nm-thick silicon film has a uniform doping concentration of 10^{17} cm^{-3} that ensures full depletion of the body and results in a 0.2-V threshold voltage [4]. A high-speed experimental setup was used to measure the transient delay response. A pulse generator is connected to the gate of the device through a coaxial cable (transmission line) and the source is grounded. The drain terminal is connected to an oscilloscope through another coaxial cable. The supply voltage is applied to the drain through a bias tee connected to the transmission line. Fig. 1 shows the output transient response to a falling input step for devices with three different gate lengths (0.4, 0.75, and 1.25 μm). Both the gate signal amplitude and the supply voltage V_{DD} are 2.5 V. The transient output signal of the 0.4-μm device exhibits a pronounced voltage overshoot while the 0.75-μm device is less affected. In contrast, the 1.25-μm device remains free of any anomalous dynamic effect. This overshoot was not observed on SOI p-MOSFET's because the generation of electron–hole pairs is weaker when triggered by energetic holes. However, it might exist for very short devices. Bulk devices were also free of the voltage overshoot.

III. Modeling

The intrinsic and extrinsic (pad) capacitances, as well as the coaxial cable of characteristic impedance $Z_0 = 50\ \Omega$, constitute the load at the drain terminal. When the MOS device is turned off, the corresponding current $I_D(t)$ decreases and, according to transmission line theory [5], the voltage at the drain terminal increases to $V_{DD} + Z_0 \cdot |\Delta I_D(t)|$ as long as no reflection occurs. The typical input signal fall time was 200 ps and the pulse duration was on the order of 1 ns. These two characteristic times, smaller than the transmission line delays, allow any reflection problems to be circumvented. Under these conditions, Fig. 2 represents the measured I_D–V_{DS} characteristics of the 0.4-μm SOI transistor together with the corresponding dynamic load line of the coaxial cable. During the switching process, the operating point moves from point A (steady state before turn-off) to point B as the gate voltage drops from 2.5 to 0 V. However, this interpretation is inconsistent with the output waveform of Fig. 1, since Fig. 2 predicts a monotonic increase of the drain voltage as the gate bias decreases. Circuit simulations including the charge dynamics of the MOS transistor, junction and pad capacitances also failed to reproduce the anomalous output voltage overshoot. An examination of Fig. 2 shows that the final operating point B is located in a region of the I_D–V_{DS} characteristic where avalanching, related to the parasitic bipolar action, occurs. This, along

Manuscript received September 9, 1992; revised January 25, 1993.

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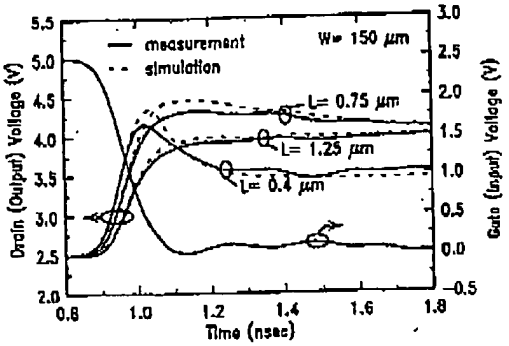

Fig. 1. Output transient signals in response to a falling input pulse. Three different gate lengths are considered.

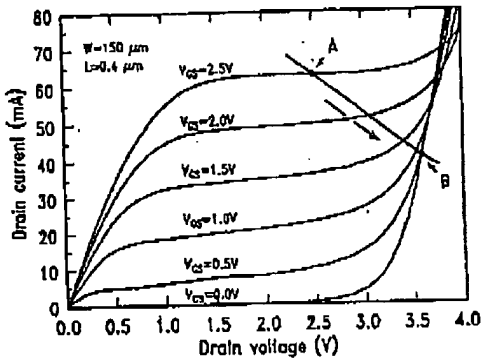

Fig. 2. Measured I_D–V_{DS} characteristics for the shorter device (L_{gate} = 0.4 μm). The dynamic load line due to the transmission line is represented.

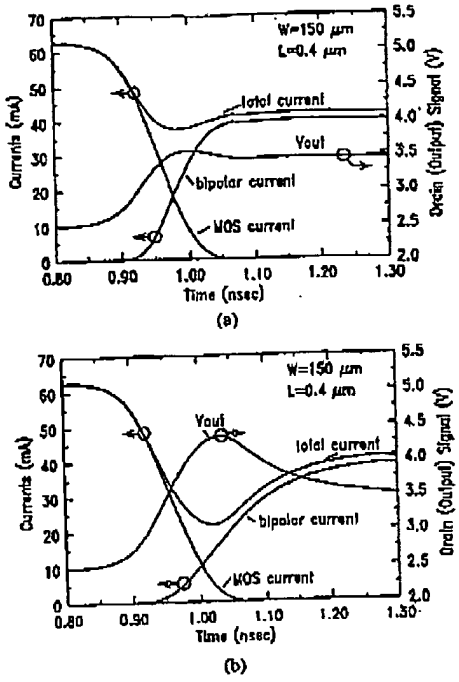

Fig. 3. Simulated total drain–source current and its two main components I_{CH} and I_C (MOS and bipolar currents) as well as the output signal: (a) without bipolar charge dynamics, and (b) with bipolar diffusion capacitance.

with the aforementioned unsuccessful attempts to simulate the overshoot, suggests that the charge dynamics of the parasitic bipolar transistor may be important. Avalanching is related to the floating-base bipolar transistor action and the positive feedback it implies: holes generated by impact ionization lower the potential barrier and increase the separation of the quasi-Fermi levels at the source–body junction, in the back interface region (body–buried-oxide interface). The subsequent base current amplification gives rise to a regenerative enhancement of impact ionization [2]. This mode of operation requires accurate modeling of both the MOS and bipolar currents. In order to take into account the fully depleted thin film of the SOI device, the static drain current is modeled similarly to [6], with enhancements to account for short-channel effects [7], [8]. The parasitic bipolar emitter–collector (source–drain) current is described by the conventional Gummel–Poon relations [9]. The body–source junction current characteristic determines the floating body–source forward bias V_{BS}, and this current takes both body–source injection and space-charge recombination currents into account. The weak impact ionization current I_{II} is self-consistently included as $I_{II} = (M - 1)(I_{CH} + I_C)$ [2], where M is the multiplication factor, I_{CH} is the MOS channel current, and I_C is the parasitic bipolar collector current. The charge-based model described in [6] was used for the transient operation of the MOS transistor. Since bipolar currents become more important for higher values of V_{DS}, the charge dynamics of the parasitic bipolar structure can be included through the following charge control relations [9]:

$$I_B = \frac{Q_F}{\tau_{BF}} + C_{dBS}\frac{dV_{BS}}{dt} \tag{1}$$

$$I_C = \frac{Q_F}{\tau_F}. \tag{2}$$

where I_B is the parasitic base current and C_{dBS} is the base–emitter (body–source) diffusion capacitance given by

$$C_{dBS} = \frac{dQ_F}{dV_{BS}} = \tau_F\frac{dI_C}{dV_{BS}}. \tag{3}$$

The junction capacitance charging currents were not considered in (1) and (2) but were included in the description of the MOS charge dynamics.

IV. Results and Discussion

The simulated output transient responses are presented by the dashed curves in Fig. 1. Good agreement is obtained for the three relevant device lengths. To demonstrate the model utility, Fig. 3(a) and (b) shows a comparison between simulations that neglect or incorporate the bipolar diffusion capacitance, respectively. The total drain-to-source current and its two main components I_{CH}

and I_C are represented. As V_{GS} decreases, the channel MOS current is reduced, resulting in an increase of the output voltage that gives rise to impact ionization and subsequent parasitic bipolar current (I_C). It is clearly shown that the voltage overshoot is directly related to the total current variations and consequently to the timing between I_{CH} and I_C. In Fig. 3(a), where the bipolar charge dynamics was not considered, the bipolar current increase compensates the falling channel current so that no pronounced voltage peak is observed. Accounting for the diffusion capacitance as in Fig. 3(b), a large part of the base current I_B is used to accommodate the change in the base charge storage $C_{dBS}\ dV_{BS}/dt$ during transient. The delayed onset of the collector current gives rise to a significant depression in the total current that explains the output voltage overshoot. On the other hand, the overshoot sensitivity to the device length exhibited in Fig. 1 can be explained by the corresponding decrease of the parasitic collector current. According to (1)–(3), dynamic changes in base charge storage become less important, as in the case of the 0.75-μm device, or completely disappear for a negligible parasitic bipolar action, as in the case of the 1.25-μm device. Consistent with Fig. 2, it is worth noting that the overshoot will disappear for a lower supply voltage when the final operating point B is out of the avalanche region, as must be the case for practical circuit design.

In summary, a voltage overshoot effect observed during SOI n-MOSFET turn-off has been reported and explained by considering impact ionization and the subsequent parasitic bipolar amplification. The inclusion of the bipolar charge dynamics proved to be essential for accurate modeling of the anomalous output response of the 0.4-μm device.

ACKNOWLEDGMENT

The authors wish to acknowledge M. M. Bierbaum and L. L. Geppert for help in setting up the high-speed measurement system, and S. E. Laux and S. Tiwari for valuable comments on the manuscript.

REFERENCES

[1] J. P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. Norwell, MA: Kluwer Academic, 1991.

[2] J. Y. Choi and J. G. Fossum, "Analysis and control of floating-body bipolar effects in fully-depleted submicrometer SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 38, pp. 1384–1391, June 1991.

[3] J. Y. Choi, "Modeling and simulation of the fully depleted SOI MOSFET for submicron CMOS IC design," Ph.D. dissertation, Univ. of Florida, Gainesville, 1991.

[4] G. Shahidi *et al.*, "Fabrication of CMOS on ultrathin SOI obtained by epitaxial lateral overgrowth and chemical-mechanical polishing," in *IEDM Tech. Dig.*, Dec. 1990, pp. 587–590.

[5] P. Grivet, *The Physics of Transmission Lines at High and Very High Frequencies*. New York: Academic, 1970.

[6] H. K. Lim and J. G. Fossum, "A charge-based large-signal model for thin film SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 446–457, Feb. 1985.

[7] S. Veeraraghavan and J. G. Fossum, "A physical short-channel model for the thin-film SOI MOSFET applicable to circuit CAD," *IEEE Trans. Electron Devices*, vol. 35, pp. 1866–1875, Nov. 1988.

[8] G. Merckel, J. Borel, and N. Z. Cupcea, "An accurate large-signal MOS transistor model for use in computer-aided design," *IEEE Trans. Electron Devices*, vol. ED-19, pp. 681–690, May 1972.

[9] H. C. de Graaff and F. M. Klaassen, *Compact Transistor Modelling for Circuit Design*, S. Selberherr, Ed. New York: Springer-Verlag, 1990.

IEEE ELECTRON DEVICE LETTERS, VOL. 16, NO. 11, NOVEMBER 1995

(2)

On the Transient Operation of Partially Depleted SOI NMOSFET's

Jacques Gautier and Jack Y.-C. Sun

Abstract—**The transient operation of partially depleted (PD) Silicon-On-Insulator (SOI) NMOSFET's is investigated, based on two-dimensional numerical simulations. The studied devices have a gate length of 0.2 μm and a floating body. They are designed for a supply voltage of 2 V. In the case of gate transient, we show that the body voltage is more influenced by the capacitive coupling with the gate electrode than the impact ionization current. Further, we demonstrate, for the first time, that the anomalous subthreshold slope, that exists in a dc static transfer I-V curve, doesn't exist in fast transient mode because the minimum time constant for body charging by impact ionization current is on the order of 3 ns in such devices.**

I. Introduction

In the case of partially depleted (PD) Silicon-On-Insulator (SOI) NMOSFET's, if there is no body contact, the body-to-source potential, V_{BS}, at a given bias results from a balance between thermal and impact ionization generations near the drain and recombination near the source. The main consequences of V_{BS} variations are changes of the threshold voltage, V_T, through the body effect, and possible turn-on of the parasitic NPN bipolar junction transistor. In the case of dc operation, this results in the well known kink effect and in the existence of a subthreshold slope improvement known as "anomalous subthreshold slope" [1] or "supra ideal subthreshold slope" when it is less than the theoretical 60 mV/decade at room temperature. This last point led to the belief that it may increase the speed of circuits, because it is equivalent to a low V_T for the drivability, but without the penalty for the leakage drain current at $V_{GS} = 0$ V that would result from a conventional reduction of V_T [2]. However, with an experimental approach, it is difficult to separate the observed improvement among different contributions: subthreshold slope improvement, average threshold voltage, kink effect, transient effects [3], [4], parasitic capacitances, etc.To clarify this point, we have adopted a theoretical approach based on the use of a two-dimensional numerical simulator FIELDAY II [5]. This tool solves Poisson's and drift diffusion equations in dc or transient modes. The impact ionization current results from a consistent resolution of the electron hydrodynamic equation to get the electron temperature, which is further used in the Scholl/Quade model [6]. Since the impact ionization current is strongly dependent on the electron energy relaxation time, τ_ϵ, a calibration procedure was initially performed to get reliable conclusions. For all the simulations, this parameter has been set to 0.15 ps after comparison of the impact ionization multiplication factor to experimental data from bulk devices (for a very close channel length and for the same biasing range) and to other simulations results (on the same SOI device) obtained with other calibrated models [7], [8]. FIELDAY II simulations were done with band-gap narrowing, Auger recombination, and SRH recombination/generation with doping-dependent lifetime $\tau = \tau_0/(1 + N/7 \times 10^{15}\ \mathrm{cm}^{-3})$, with $\tau_0 = 1\ \mu$s for electron and hole carriers.

Manuscript received April 17, 1995; revised July 26, 1995.

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II. Simulations and Discussion

In this study, we have simulated PD-SOI NMOSFET's with a LDD structure. The gate length is 0.2 μm, the gate oxide thickness is 5 nm and the silicon film thickness is 100 nm with a uniform p-type doping of 4.5×10^{17} cm^3. The buried oxide thickness is 0.4 μm. There is no body contact, so the body is floating.

In a first set of simulation, we consider a transient gate voltage increase with a slew rate of 100 ps/V for a constant drain voltage of 2 V. This corresponds to the switching on of a NMOS transistor in an inverter, where the drop of output voltage is delayed compared with the rise of input voltage. In weak inversion, a linear ramp of V_{GS}, would lead to a displacement current stronger than the quasistatic channel current and make it impossible to compare with dc simulations. In order to overcome this, we used a staircase gate voltage ramp, i.e., small linear ramps of V_{GS} by increments of 0.1 V in 2 ps, followed by constant V_{GS} steps of 8 ps, that is an average increase with a slew rate of 100 ps/V (Fig. 1). During the constant V_{GS} steps, there is no displacement current and we verified that 8 ps is sufficient to terminate the channel transient and the displacement of charge in the body. So, at the end of each V_{GS} step, we got the intrinsic drain current without the contribution of any displacement current. The plotting of this current versus the corresponding V_{GS} gave the transient subthreshold characteristics, which is compared with the dc one in Fig. 2. We observe that the dc anomalous subthreshold slope doesn't exist in the transient mode. In fact, we get a slope of 75-mV/decade instead of 45 mV/decade. Fig. 3 shows the corresponding variations of the transient and dc body potential versus V_{GS}. This body potential was extracted from the two-dimensional distributions of hole and electron quasifermi potential on the source edge of the body, at the back interface $V_{BS} = QF_P - QF_N$. Proceeding this

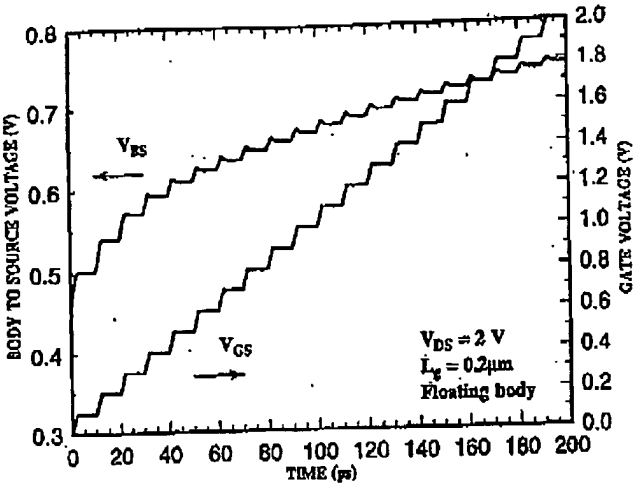

Fig. 1. Gate voltage waveform for decoupling the intrinsic SOI transient effects from the displacement current and time dependence of the body potential for increasing the gate voltage from 0 V to 2.5 V, in increments of 10 ps.

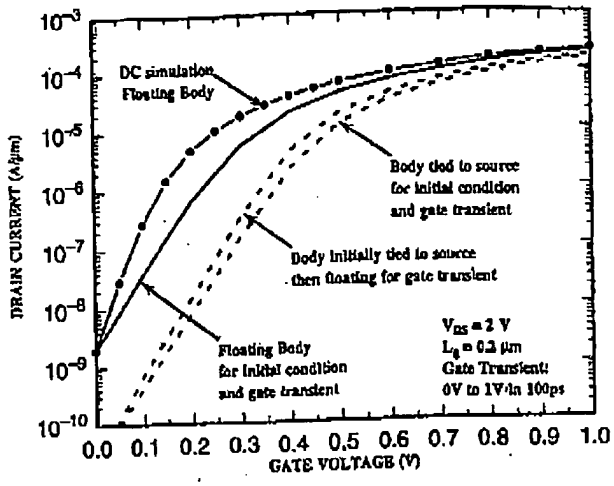

Fig. 2. Simulated subthreshold characteristics of a partially depleted NMOSFET. In the case of a gate transient, for comparison with the dc regime, only the intrinsic contribution of the drain current is plotted, i.e., value at the end of each incremental V_{GS} step. In solid line, the body is floating. In dashed line, a body contact has been used to tie the body to the source, either for the initial condition and during the transient, or only for the initial condition, leaving it floating during the transient.

way avoids any perturbation that could otherwise occur, for instance in using a floating body contact. For V_{DS} = 2 V, we see that the transient body potential is lower than the dc value for almost all the V_{GS} range, which means that, for this timing of the transient, the impact ionization current is not strong enough to increase the body charge to the dc level in phase with the V_{GS} biasing. This is confirmed by performing the same transient simulation, from the same initial dc solution, but turning off the impact ionization in FIELDAY during the transient. In fact, other simulations show that the time, for only charging the body by impact ionization, from a V_{BS} = 0 V initial condition (set by a body contact which is then left floating) and a constant V_{GS} and V_{DS} biasing, is at least 3 ns for V_{DS} = 2 V. This is the minimum value corresponding to the peak of the impact ionization current for V_{GS} close to the threshold voltage. In Fig. 3, we have also plotted the results of another set of simulation for which V_{GS} is decreased from 2.5 V to 0 V in incremental steps with an average slew rate of −100 ps/V. Since the impact ionization current, and also V_{BS} in dc mode, are maximum for a low V_{GS}, one would expect also an increase of V_{BS} in transient mode when V_{GS} is decreased slowly. Instead, we got a decrease, which confirms that the impact ionization doesn't play a dominant role. Noting that in transient mode V_{BS} varies the same way as V_{GS}, a capacitive coupling between the body and the gate is expected.

In Fig. 1, the V_{BS} variation versus time, for V_{GS} increasing (staircase voltage ramp), is plotted. There is an obvious correlation between the body voltage and gate voltage variations, which is in agreement with the dominant role of a body to gate capacitive coupling. Such a coupling is known to induce a transient increase of V_{BS}, resulting in a drain current overshoot at low drain voltage [9]. Below the threshold voltage, $V_T \sim$ 0.4 V, there is a direct gate to body capacitance that explains the coupling. Above V_T (i.e., above 40 ps for this simulation), the rate of increase of V_{BS} is lower than before V_T, but it is not negligible. However, one expects an electrostatic shielding by

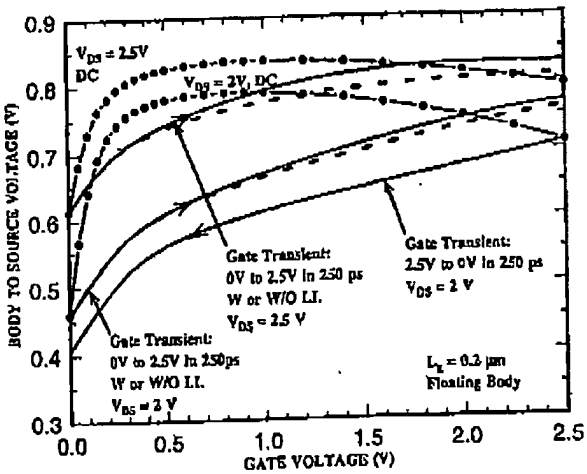

Fig. 3. Variations of the body potential versus the gate voltage for dc or transient simulations. V_{GS} increasing or decreasing with an average slew-rate of 100 ps/V. In dashed line, simulation with impact ionization turned off for the V_{GS} increasing transient, not for the initial dc at V_{GS} = 0 V.

In Fig. 4, we show the edge of the body space charge layer for different gate voltages, corresponding to the V_{GS} increase transient simulation. There is a hole redistribution in the body, without significant increase of the total charge, which also means a low influence of the impact ionization generation during this transient. As discussed previously, there are two regimes of the gate to body coupling.

1) Between 0 V and 0.4 V, subthreshold regime, the increase of the depletion region, under the gate, corresponds to the surface band-bending increase along the entire channel.

2) Between 0.4 V and 2 V, saturation regime, there is a [illegible] the

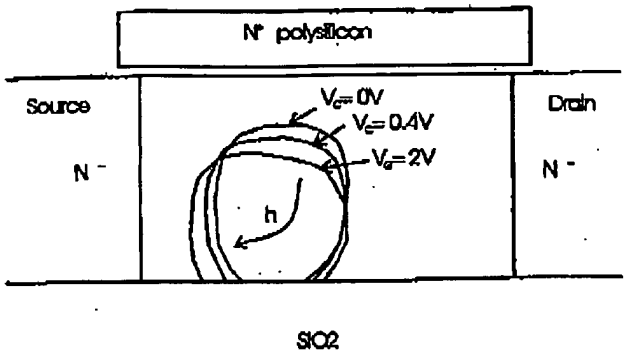

Fig. 4. Changes of the body space charge layer for a transient increase of the gate voltage from 0 V to the threshold voltage, then to 2 V, showing increasing forward biasing of the body-source diode. The drain voltage is 2 V.

channel. However, for increasing V_{GS}, this variation becomes more and more linear, thus, the surface band-bending is increasing between source and drain (not near the source where it is clamped to $2\Phi_F - V_{BS}$). The corresponding depletion charge increase, resulting from the V_{GS} increase, is equivalent to a gate-body capacitive coupling. In other words, the electrostatic channel shielding exits near the source, but not near the drain because the device is in saturation regime.

To emphasize the advantage of floating body operation, simulations have also been performed with the body tied to the source, either for the initial condition and during the transient, or only for the initial condition, leaving it floating during the transient. Fig. 2 shows that, in addition to the initial shift of V_T, the dynamic change of V_{BS} contributes to an increase of the drain current through a dynamic reduction of V_T.

III. Conclusion

Based on numerical simulation, we demonstrate, for a low supply voltage, e.g., 2 V in our study, that the impact ionization current doesn't significantly contribute to a dynamic change of the threshold voltage, because the impact ionization current is not high enough to change the body charge during the gate switching. Consequently, the dc sub-60 mV/decade subthreshold slope of partially depleted device, known as anomalous subthreshold slope, doesn't exist in transient mode. There is however a dynamic change of the body potential by the gate to body capacitance coupling, which only exists in SOI and does help the switching performance of SOI devices.

Acknowledgment

The authors thank S. Furkay and G. Fiorenza for support in using FIELDAY II simulator and B. Davari and J. Hartmann for management support.

References

[1] J. Fossum, *et al.*, "Anomalous subthreshold current-voltage characteristics of n-channel SOI MOSFET's," *IEEE Electron Device Lett.*, vol. EDL-8, no. 11, pp. 544–546, Nov. 1987.

[2] G. Shahidi, *et al.*, "A room temperature 0.1 μm CMOS on SOI," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2405–2412, 1994.

[3] C. Leroux, J. Gautier, and M. Spalanzani, "Parasitic transients induced by floating substrate effect and bipolar transistor on SOI technologies," in *Microelectronic Engineering 15*. Amsterdam: Elsevier, 1991, pp. 199–202.

[4] D. Suh and J. Fossum, "Dynamic floating-body instabilities in partially depleted SOI CMOS circuits," *IEDM Tech. Dig.*, pp. 661–664, Dec. 1994.

[5] S. Furkay, *et al.*, *"FIELDAY II User's Manual*, Version no. 7.3.0," IBM Technology Modeling, East Fishkill, NY, 1993.

[6] E. Scholl and W. Quade, "Effect of impact ionization on hot-carrier energy and momentum relaxation in semiconductors," *J. Phys. C*, vol. 20, pp. L861–L867, 1987.

[7] K. K. Thornber, "Application of scaling to problems in high-field electronic transport," *J. Appl. Phys.*, vol. 52, pp. 279–290, 1981.

[8] M. V. Fischetti, "Monte Carlo simulation of transport in technologically significant semiconductors of the diamond and zinc-blend structures-Part I Homogenous transport," *IEEE Trans. Electron Devices*, vol. 38, pp. 634–649, 1991.

[9] K. Kato and K. Taniguchi, "Numerical analysis of switching characteristics in SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-33, no. 1, pp. 133–139, 1986.

Proceedings 1994 IEEE International SOI Conference, Oct. 1994

PHYSICAL MODELING OF BENEFICIAL DYNAMIC FLOATING-BODY EFFECTS IN NON-FULLY DEPLETED SOI CMOS CIRCUITS

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The floating-body configuration is desirable in scaled SOI CMOS technology because of area efficacy. Unfortunately it portends various problems, one of which is the premature parasitic-BJT breakdown [1] that occurs in both fully depleted (FD) and non-fully depleted (NFD) SOI MOSFETs. In the NFD device, other floating-body effects [2]-[4], some of which can be beneficial, are apparent at drain-source voltages below the breakdown because of the sensitivity of threshold voltage to the body-source bias. This bias, which can be forward or reverse in dynamic operation of the MOSFET, is due to positive or negative excess majority-carrier densities in the floating body. In this paper, we present a physical model for the NFD/SOI MOSFET and use it in a circuit simulator (SOISPICE) to identify and assess beneficial floating-body effects in dynamic operation of scaled CMOS digital circuits.

Our model, an evolution of the TFA formalism in [5], physically accounts for the aforementioned floating-body effects in the short-channel device. Underlying these accountings is the characterization of the body bias V_{BS}, which is defined by the carrier recombination and generation currents inherent in the device, as well as by the body charge dynamics. The model has been verified by numerical device simulations, and by measured current-voltage data as exemplified in Fig. 1 for a 0.2-μm NFD test device. Note in Fig. 1(b) that the model predicts well the supra-ideal subthreshold slope for high V_{DS}, which results from a floating-body effect driven by impact-ionization charging of the body [3] and dependent on the nonideality of the source-body junction recombination characteristic (but independent of the parasitic BJT). SOISPICE CMOS circuit simulations show clearly however that this effect is not beneficial to speed [6], but only increases static power as implied by the off-state currents indicated in the figure.

Nonetheless the speed of a floating-body NFD/SOI CMOS circuit is inherently faster than that of a body-tied-to-source circuit, especially for low supply voltage as exemplified by the SOISPICE-predicted inverter propagation delays plotted in Fig. 2. All the (three-stage inverter chain) simulations were done with identical model parameters. The underlying beneficial floating-body effect results from $V_{BS} > 0$ driven by body charging due to thermal carrier generation, even at low V_{DS}. This speed improvement would seem to imply a common design tradeoff, however, because it results from effective threshold lowering which would also increase off-state current and hence static power. The transient circuit simulations suggest though that this tradeoff is not needed; they show that the benefit is not undermined by increased off-state current because of a unique dynamic floating-body effect in the NFD/SOI MOSFET. As indicated by the SOISPICE-predicted transient currents in the CMOS inverter chain, plotted in Fig. 3 for floating and tied bodies, the off-state current is effectively suppressed when the body is floating. The reason for this suppression is that the body is partially depleted of majority carriers in the on state, and the need to recover them in the off state produces a negative V_{BS}. Whereas the time constant associated with this recovery in the tied-body device (i.e., the dielectric relaxation time) is negligibly short, that for the floating-body device (i.e., a carrier generation lifetime) is very long compared to operating periods of high-frequency signals in scaled CMOS circuits. Thus $V_{BS} < 0$ is maintained during the off-state period of the floating-body device, and the current is suppressed because of the implied higher threshold. The static power in the circuit is thereby effectively decreased, even though the V_{BS}-induced threshold lowering is being exploited in the on state. Note that the dynamic floating-body benefits are hysteretic; every cycle is somewhat different. Hence exploitation of the beneficial effects will necessitate device/circuit design scrutiny.

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Acknowledgments

This work was supported by Texas Instruments. We thank IBM for measured test device data.

References

[1] K. K. Young, et al., IEEE Trans. Electron Devices, vol. ED-35, pp. 426-431, Apr. 1988.
[2] J.-P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI. Boston, MA: Kluwer, 1991.
[3] J. G. Fossum, et al., IEEE Electron Device Lett., vol. EDL-8, pp. 544-546, Nov. 1987.
[4] H. K. Lim, et al., IEEE Trans. Electron Devices, vol. ED-31, pp. 1251-1258, Sept. 1984.
[5] S. Veeraraghavan, et al., IEEE Trans. Electron Devices, vol. ED-35, pp. 1866-1875, Nov. 1988.
[6] J. G. Fossum, et al., ECS '94 Symp. on SOI Technology and Devices, May 1994.

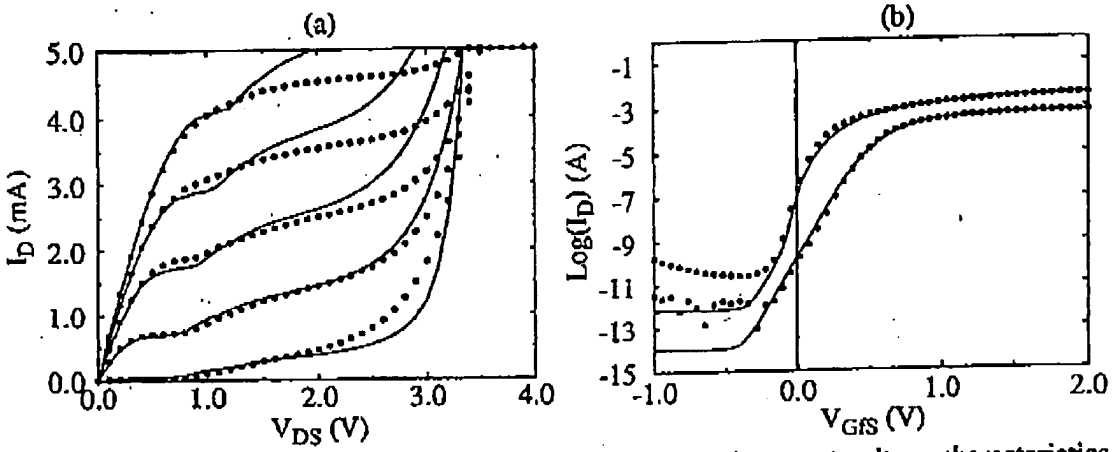

Fig. 1. Measured (points) and SOISPICE-simulated (curves) current-voltage characteristics of a scaled floating-body NFD/SOI MOSFET; L = 0.2 μm. In (a), V_{GfS} varies from 0.5 to 2.5 V, and in (b), V_{DS} is 0.1 V and 2.0 V, the latter for which S = 44 mV.

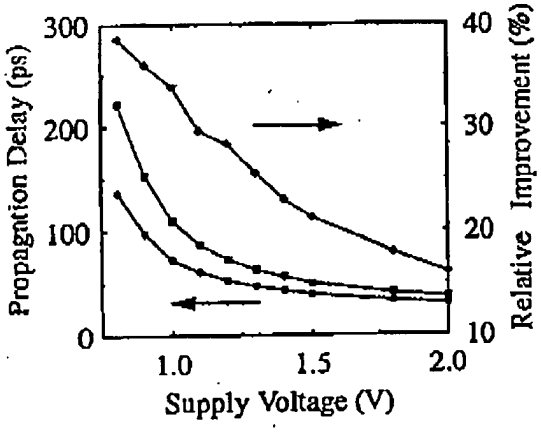

Fig. 2. SOISPICE-predicted NFD/SOI CMOS inverter propagation delay (per gate) versus V_{DD} for floating (●) and tied (■) bodies, and the relative speed enhancement afforded by the floating body; L = 0.2 μm.

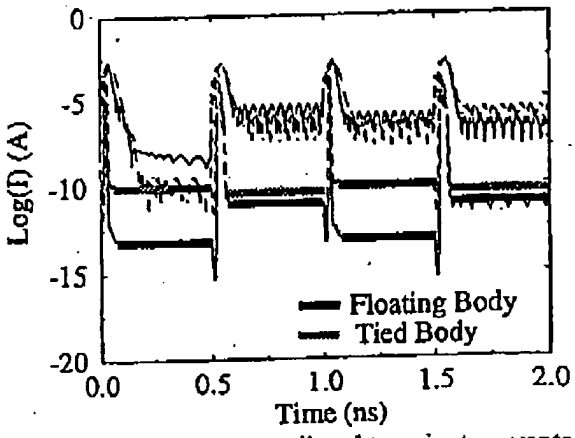

Fig. 3. SOISPICE-predicted transient currents in the NFD/SOI CMOS inverter chain, with floating and tied bodies; L = 0.2 μm, V_{DD} = 1.5 V. The physical off-state leakage (channel) currents are highlighted; the noisy currents reflect errors associated with the integration method used in SPICE.

Is hard to calibrate PD parameters

(4)

Dynamic Floating-Body Instabilities in Partially Depleted SOI CMOS Circuits

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Abstract

Dynamic floating-body instabilities in PD/SOI CMOS devices and circuits are investigated using a physical yet compact MOSFET model in SOISPICE. SOISPICE simulations show how some floating-body effects can be beneficial, but they reveal that the hysteretic nature of the effects causes instabilities. They further exemplify how floating-body charge dynamics can complicate model parameter extraction. Accordingly SOISPICE-aided examinations of SRAM and DRAM circuits imply that conservative designs will be necessitated in PD/SOI technology.

Introduction

The floating-body configuration is desirable in scaled SOI CMOS technology because of area efficacy. Unfortunately it portends various problems, one of which is the premature parasitic-BJT breakdown [1]. In the partially depleted (PD) SOI MOSFET, additional DC floating-body effects [2], [3] (e.g., current kinks) are apparent at drain-source voltages below the breakdown because of the sensitivity of threshold voltage to the body-source bias (V_{BS}), which is governed by free-carrier charging of the body. These effects are compounded in dynamic device/circuit operation by transient charging currents that define $V_{BS}(t)$, which can be positive or negative. In this paper we examine these dynamic floating-body effects using a physical yet compact model for the PD/SOI MOSFET [4] implemented in SOISPICE [3]. SOISPICE device/circuit simulations show some performance benefits afforded by the effects, but they also reveal circuit instabilities and even complications in model parameter extraction caused by them.

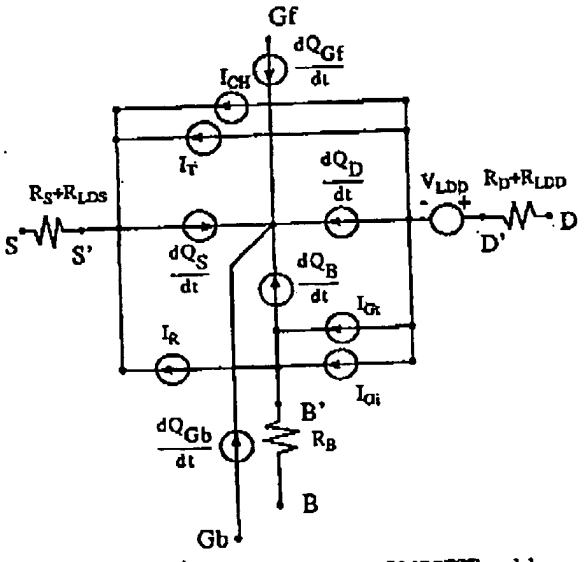
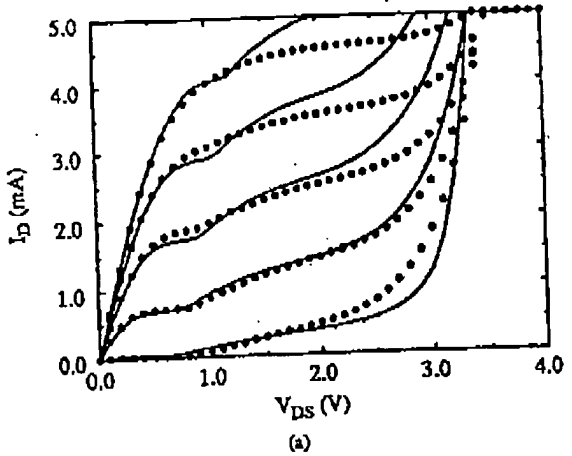


Fig. 1. Network representation of the PD/SOI MOSFET model.

Model Utility

Our PD/SOI MOSFET model is charge-based and physically formulated as reflected by the network representation in Fig. 1. The floating body is a model option, for which $V_{BS}(t)$ is properly characterized by the nodal equation involving dQ_B/dt (body charging current) as well as



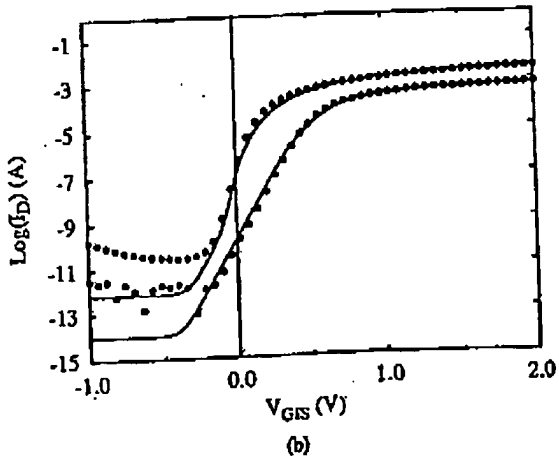


Fig. 2. Measured (points) and SOISPICE-simulated (curves) I-V characteristics of an L = 0.2-μm floating-body PD/SOI MOSFET. In (a) V_{GS} varies from 0.5 to 2.5 V, and in (b) V_{DS} is 0.1 V and 2.0 V.

same with I/I

I_R (source-body junction recombination current), I_{GI} (thermal generation current), and I_{Gi} (impact-ionization current). The model has been verified by numerical device simulations as well as device I-V measurements. The latter are exemplified in Fig. 2 for a 0.2-μm floating-body n-channel MOSFET. Because of the physical nature of the model, no rigorous parameter optimization was needed for these SOISPICE simulations. The parameters were evaluated from the known device structure; only minor tuning, e.g., for the mobility and its degradation factor, was used. The model prediction is generally good, even for the high-V_{DS} subthreshold- and saturation-region kinks, the former of which is reflected by the supra-ideal slope (S = 44 mV) in Fig. 2(b).

Note in Fig. 2(a) however that there are significant model-measurement discrepancies in high-power regions due to self-heating (which is not modeled) affecting the measured data [5]. Since the self-heating is mainly a DC effect, model parameters for (digital) circuit simulation must be evaluated without it. Thus conventional parameter optimization/extraction cannot be done. Recently a pulsed I-V measurement method was proposed [6] to avoid self-heating. However, although unacknowledged, this method can be undermined by dynamic floating-body charging effects as exemplified in Fig. 3. The SOISPICE-predicted transient drain current for gate and drain voltage pulses with widths (nanoseconds) comparable to those used in [6] shows that the current might not reach its static level, and hence the parameter values extracted could be invalid. The delay is the time required for generated (e.g., via impact ionization) carriers to charge the body. It depends on the device structural and electrical properties, and hence proper voltage pulse widths are not readily apparent.

Floating-Body Benefits

The speed of a floating-body PD/SOI CMOS circuit is inherently faster than that of a body-tied-to-source circuit,

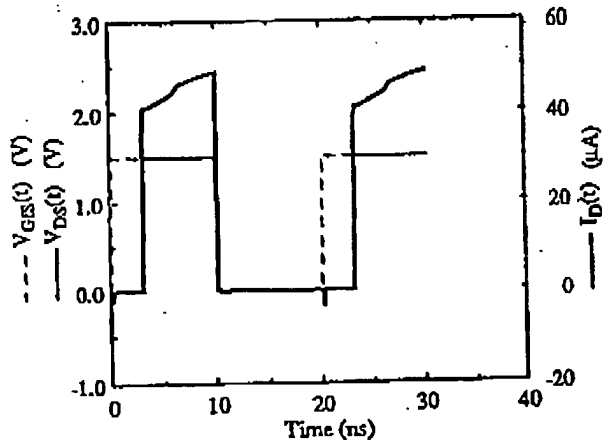


Fig. 3. SOISPICE simulation of a pulsed I-V measurement on a floating-body PD/SOI MOSFET.

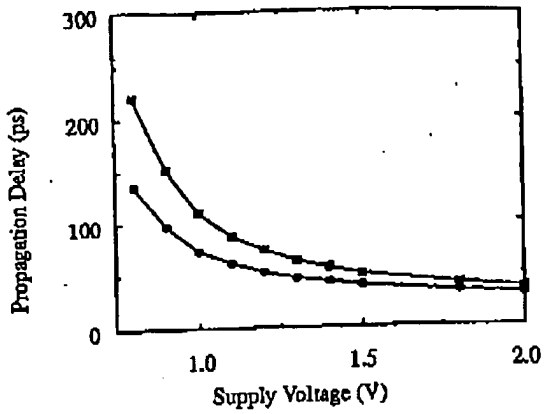


Fig. 4. SOISPICE-predicted PD/SOI CMOS inverter propagation delay (per gate) versus V_{DD} for floating (●) and tied (■) bodies; L = 0.2 μm.

especially for low supply voltage (V_{DD} below the kink voltage), due to thermal generation-driven body charging ($I_{GI} - I_R \rightarrow V_{BS} > 0$ for n-channel MOSFET) and threshold lowering. This benefit, revealed by SOISPICE-predicted propagation delays in inverter-chain circuits exemplified in Fig. 4, is potentially viable because of the dynamic suppression of the off-state current as shown by the simulation results in Fig. 5. The suppression occurs because the MOSFET body is partially depleted of majority carriers in the on state, and the depletion charge in the off state forces $V_{BS}(t) < 0$ as the carriers are recovered (by thermal generation). Since the time for full recovery in the floating-body device is long relative to typical signal periods in fast CMOS circuits, the implied higher threshold voltage is maintained during the off-state period, and the current is effectively suppressed. SOISPICE-simulated $V_{BS}(t)$ in Fig. 6 for n-channel MOSFETs in the inverter chain supports this insight.

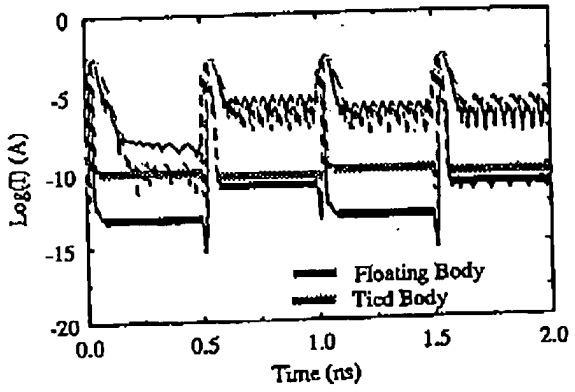


Fig. 5. SOISPICE-simulated transient currents in the PD/SOI CMOS inverter chain with floating and tied bodies; L = 0.2 μm, V_{DD} = 1.5 V. The physical off-state currents are highlighted; the noisy currents reflect errors associated with the integration method used in SPICE.

Ghavam: diff. from Keith Jenkins meas

27.6.2

Vt recovery time much diff. for on + OFF state

NM reduced by hysteresis (not like Schmitt)

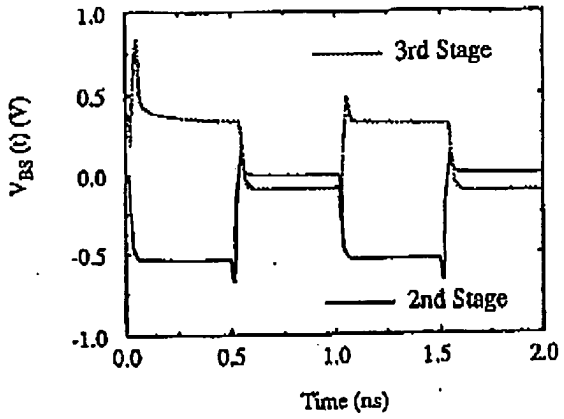


Fig. 6. SOISPICE-simulated transient body-source voltage of n-channel MOSFETs in the PD/SOI CMOS inverter chain.

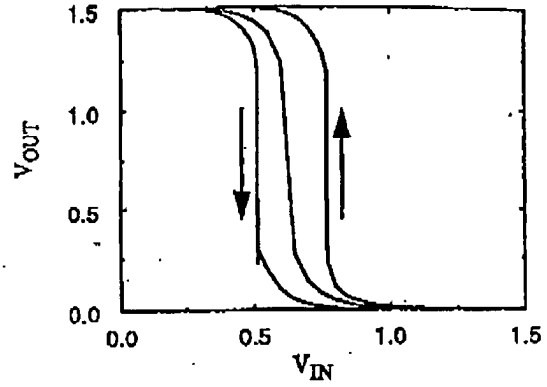


Fig. 8. SOISPICE-simulated forward- and reverse-swept (slow-)transient voltage-transfer characteristics of a floating-body PD/SOI CMOS inverter. The steady-state characteristic is shown for comparison.

Hysteresis

The dynamic floating-body benefits are however hysteretic, depending on the history of the device charge condition as evident in Figs. 5 and 6. The hysteresis in device characteristics is clearly reflected in Fig. 7 by the SOISPICE-simulated transient threshold voltage of an n-channel PD/SOI MOSFET corresponding to different gate-voltage pulses. Even though the steady-state threshold voltages (defined by the preliminary DC solution for transient analysis in SOISPICE) are identical, different initial body charge conditions, dependent on the applied gate voltage, dictate the different threshold voltage variations in time since they define the transient $V_{BS}(t)$. Recovery times are also dependent on the sign of $V_{BS}(t)$; the transient process of depleting the body (via carrier recombination) depends on the forward-bias characteristics of the source-body junction, and is generally faster than that of replenishing it (via carrier generation) which depends on the reverse-bias characteristics. When the gate bias is switched in finite time, the recovery is slowed because of counteracting (recombination and generation) tendencies. The hysteresis of threshold voltages is reflected in Fig. 8 where simulated transient voltage-transfer characteristics of a PD/SOI CMOS inverter are shown. The inverter input voltage was ramped up and down at a very slow rate so as to obviate the gate propagation delay, but fast enough to see the hysteretic effects defined by the recovery of the body charge. Both the forward- and reverse-swept transfer characteristics are offset from the steady-state one because of the body charging-induced lowering of the threshold voltage of the transistor being switched from off to on.

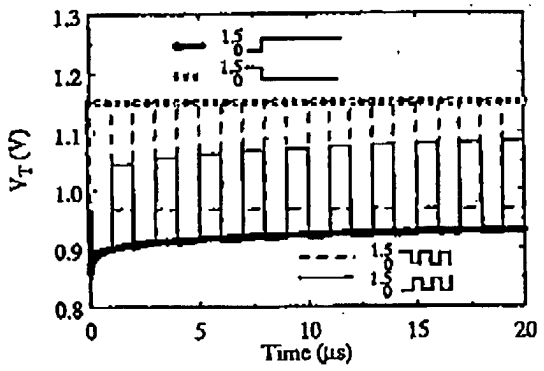


Fig. 7. SOISPICE-simulated transient threshold voltage of an L = 0.2-μm floating-body PD/SOI MOSFET corresponding to gate-voltage pulses having different initial values (0 and 1.5 V) and frequencies (0 and 500 kHz).

Design Implications

The design of circuits with PD/SOI MOSFETs must accommodate the inherent hysteresis, which otherwise can cause significant instabilities. We will exemplify the possible instabilities in SRAM and DRAM circuits using SOISPICE, and discuss the needed design tradeoffs. Obviously a CMOS SRAM built with inverters having characteristics like those in Fig. 8 would have a reduced static noise margin. For example, Fig. 9 shows predicted bit-line voltage transients corresponding to read-"0" operations of a PD/SOI CMOS SRAM cell. For the word voltage $V_W = V_{DD}$, the floating-body circuit (i) is faster than the tied-body (~bulk-Si) circuit (ii). However, when a "noisy" word voltage is used ($V_W > V_{DD}$), the floating-body circuit loses its functionality (iii), while the tied-body circuit remains stable (iv). To negate the hysteresis effect in this case, the pass transistors must be re-ratioed, which sacrifices speed (v).

DRAMs built on SOI substrates are of interest because storage capacitance can be less than in bulk-Si DRAMs due to reduced bit-line capacitance in SOI [7]. The storage capacitance can be further reduced if floating-body PD devices are used for cell transistors. Whereas V_{BS} of the bulk-Si cell transistor is fixed at a negative bias, that of the floating-body PD/SOI cell transistor is positive when the device is

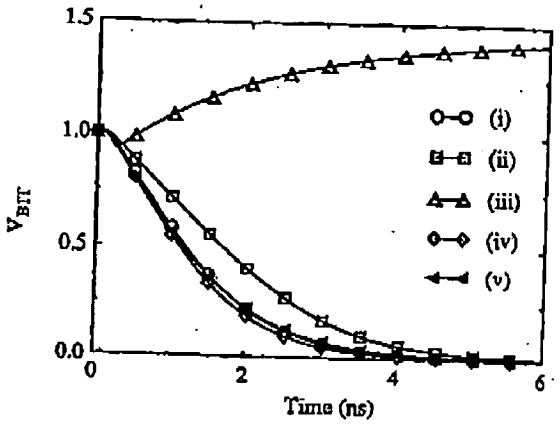


Fig. 9. SOISPICE-predicted transient bit-line voltages corresponding to read-"0" operations of a PD/SOI SRAM cell; V_{DD} = 1.5 V. The MOSFET bodies are floating for (i), (iii), and (v), and are tied for (ii) and (iv); V_W = 1.5 V for (i) and (ii), = 2.0 V for (iii), (iv), and (v); (W/L)pass = 0.3μm/0.2μm for (i), (ii), (iii), and (iv), = 0.2μm/0.2μm for (v).

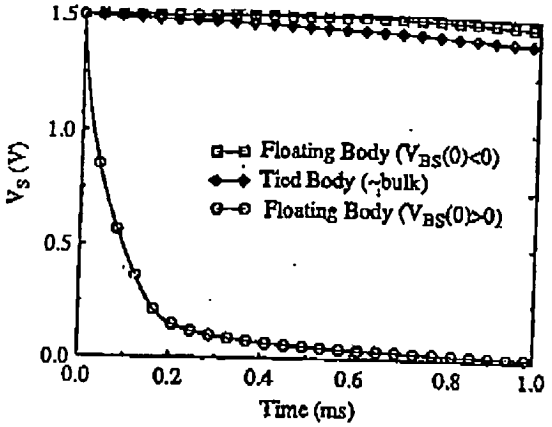


Fig. 11. SOISPICE-predicted decay of the stored data voltage in floating- (with different initial $V_{BS}(0)$) and tied-body PD/SOI DRAM cells.

turned on to write "1" on the storage node. Thus the hysteretic threshold voltage reduction allows a higher stored data voltage (V_S), as predicted by SOISPICE in Fig. 10. However this benefit also can be undermined by associated instabilities since the leakage current through the cell transistor, which defines the refresh cycle, is also affected. Fig. 11 compares the decay of the stored data voltage for floating- and tied-body (~bulk-Si) PD/SOI DRAM cells. The decay in the floating-body cell is quite sensitive to the body charge condition since it defines $V_{BS}(t)$ and the dynamic threshold voltage. Unless the charge in the floating body is controlled, e.g., via all-select reset, the PD/SOI DRAM design must be based on a worst-case refresh scenario, which, according to Fig. 11, would yield a much less than optimal memory circuit.

Conclusion

Dynamic floating-body instabilities in PD/SOI CMOS devices and circuits have been investigated using a physical yet compact MOSFET model in SOISPICE which properly characterizes the floating-body bias in transient as well as DC simulations. SOISPICE predictions reveal how floating-body charge dynamics can complicate model parameter extraction. Simulations show that the floating-body effects can be beneficial to performance, but that instabilities due to the hysteretic nature of the effects must be acknowledged in assessment and design of PD/SOI technology. Plainly the simulations imply that efficient circuit design in the technology will require a compact device model that properly accounts for the hysteresis and the unique floating-body effects. SOISPICE-aided examinations of SRAM and DRAM circuits revealed that the instabilities could preempt the beneficial effects and indeed necessitate more conservative designs than in the bulk-Si technology.

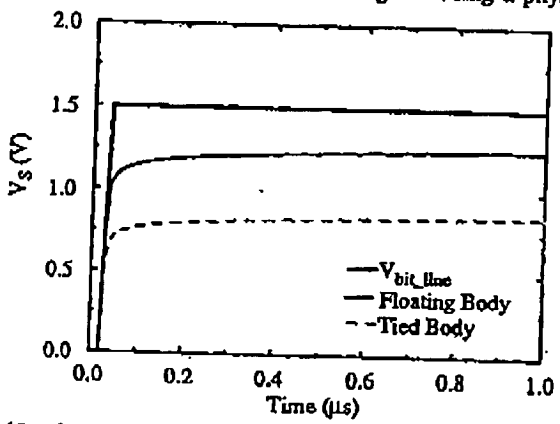


Fig. 10. SOISPICE simulations of write "1" in floating- and tied-body PD/SOI DRAM cells.

Acknowledgments

This work was supported in part by Texas Instruments and by the Semiconductor Research Corporation. We thank IBM for measured test device data.

References

[1] K. K. Young, et al., *IEEE Trans. Electron Devices*, vol. 35, pp. 426-431, Apr. 1988.

[2] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. Boston, MA: Kluwer, 1991.

[3] J. G. Fossum, et al., *Proc. 6th Internat. Symp. on SOI Technology and Devices*, ECS Vol. 94-11, pp. 447-452, May 1994.

[4] D. Suh and J. G. Fossum, submitted to *IEEE Trans. Electron Devices*, Aug. 1994.

[5] L. T. Su, et al., *IEEE Trans. Electron Devices*, vol. 41, pp. 69-75, Jan. 1994.

[6] K. A. Jenkins, et al., IEEE Internat. SOI Conf., Nantucket Island, MA, Oct. 1994.

[7] T. Eimori, et al., *IEEE IEDM Tech. Dig.*, pp. 45-48, Dec. 1993.

beneficial for DRAM? 27.6.4

more conservative design to handle V_t hysteresis reduce advantages of

refresh time init. longer, but stored data falls abruptly when $V_{BS} > 0$ PD SOI

(5)

FLOATING-BODY PROBLEMS AND BENEFITS IN FULLY DEPLETED SOI CMOS VLSI CIRCUITS

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ABSTRACT

A physical model for the fully depleted submicron SOI MOSFET is described and used to assess problems and possible benefits in SOI CMOS VLSI digital circuits that result from the parasitic bipolar junction transistor (BJT) in the floating-body device. The study shows that the problems overwhelm the benefits, and hence must be alleviated by controlling the activation of the BJT via device design tradeoffs. A feasible approach to the needed design optimization is demonstrated by device/circuit simulations.

INTRODUCTION

Fully depleted SOI CMOS is potentially competitive in deep-submicron VLSI applications because of eased scaling afforded by the variable (thin) film thickness as well as simple isolation [1]. The viability of SOI however is threatened by floating-body problems, the most annoying of which are due to the impact ionization-triggered activation of the parasitic (npn) bipolar transistor (BJT) in the (n-channel) SOI MOSFET structure (illustrated in Fig. 1). This effect, which results in loss of gate control, has been extensively analyzed at the device level under dc conditions (i.e., by examining the source-drain breakdown and subthreshold conduction), but little study of the effect and its unique repercussions has been done at the circuit level under transient conditions. Furthermore little study of the possible benefit to circuit speed afforded by the BJT activation has been done. In this paper we describe a physical model for the fully depleted SOI MOSFET, written into SPICE2 source code, and use it to assess floating-body bipolar effects in submicron SOI CMOS digital circuits and to suggest designs to control and possibly exploit them beneficially.

SOI MOSFET MODEL/SOISPICE-2

The physical device model is a major extension of our previously developed short-channel, charge-based model [2] for the thin-film SOI MOSFET. The noteworthy extensions [3] are accountings for subthreshold current at both the front and back surfaces, for LDD and LDS regions, as well as for the impact-ionization current and the parasitic BJT in the LDD/LDS device structure shown in Fig. 1. The new five-terminal (source, drain, front gate, back gate, and body, which normally floats) model is based on the assumption of a fully depleted film body, including the back surface. The analyses of the (ambipolar) carrier transport in the device structure which underlie the model require iterative numerical solution. The model is hence semi-numerical, yet is implemented effectively in SPICE2 source code creating "SOISPICE-2" [3], which enables reliable and efficient mixed-mode device/circuit simulation.

The subthreshold channel currents are modeled [3] as weak-inversion currents, constrained by V_{DS}-dependent limits and

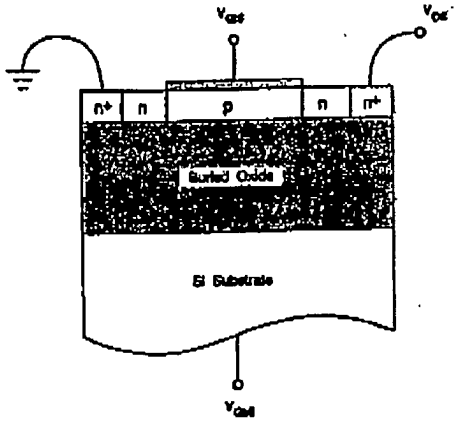

Fig. 1. Cross-sectional view of the contemporary thin-film SOI MOSFET including an LDD and an LDS.

added to the strong-inversion currents in [2]. The basic weak-inversion current expression, applied to both front and back channels, is formulated to be consistent with the physical characterizations of short-channel and gate charge-coupling effects in [2].

The characterization [3] of the (weak) impact-ionization current extends that in [2] by accounting for carrier generation in the LDD as well as in the high-field portion of the channel (where the electron velocity is assumed to be saturated), and by including the BJT (collector) current I_T and the total (front- and back-) channel current I_{CH} in the driving current:

$$I_{GI} = (M-1)(I_{CH} + I_T) \qquad (1)$$

where

$$(M-1) = \int_{L_{eff}}^{L} \alpha_0 \exp\left(-\frac{\beta_0}{E_y}\right) dy + \int_{L}^{L+L_{LDD}} \alpha_0 \exp\left(-\frac{\beta_0}{E_y}\right) dy . \qquad (2)$$

The first integral in (2) follows from [2], but with $E_y(y)$ reduced because of the voltage drop V_{LDD} across the LDD. The second term follows from $E_y(y)$ in the LDD derived from a solution of Poisson's equation that is consistent with the peak electric field as characterized by the channel analysis. The LDD analysis [3], which also yields V_{LDD}, obviously requires an iterative solution because of the close coupling to the channel analysis.

The BJT current I_T in (1) is approximated for short L via the classical integral charge-control relation:

$$I_T \simeq \frac{qW_b n_i^2 D_n}{\int_{Body} p\,dy} \left[\exp\left(\frac{qV_{BS}}{kT}\right) - 1\right] \qquad (3)$$

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where V_{BS} is the (induced) body-source forward bias, t_b is the SOI film thickness, D_n is a transverse field-dependent diffusivity, and

$$\int_{body} p\,dy \simeq \frac{L_{ef} n_i}{2} \exp\left(\frac{qV_{BS}}{2kT}\right) + L_{ef} N_A \qquad (4)$$

is the integrated majority-hole density in the body (base). The basis for (4) is an assumed linear distribution of holes across the channel region with $p \simeq n$ in the normally depleted body. Numerical device simulations [4] support this assumption for normal activation of the BJT. The last term in (4) is included to keep the model tractable when the device is off and the assumption is not applicable.

The numerical device simulations [4] further show that when the parasitic BJT is activated in the fully depleted SOI MOSFET structure, the primary recombination current I_R (viz., injected-hole removal current) is supported by the quasi-neutral source region, including the LDS. Recombination in the depleted film body tends to be small because of carrier separation by the transverse electric field and because of long carrier lifetime relative to that in the higher-doped source. Thus from a regional analysis of the hole continuity equation in the source, accounting for the longitudinal electric field supporting the electron current (I_{CH}+I_T) in the LDS, we derive [3] $I_R \propto \exp(qV_{BS}/kT)$ in terms of (I_{CH}+I_T) as well as the electrical and structural properties of the n^+-n source. This analysis, which also requires an iterative solution, yields the voltage drop across the LDS, V_{LDS}, as well. Note that the BJT current gain, $\beta = I_T/I_R$, is injection level-dependent, and can be controlled by a properly designed LDS which enhances I_R [3], [4].

The carrier-transport analyses underlying the SOI MOSFET model assume, where necessary, accepted physical models such as doping dependences of carrier mobilities and lifetimes. The charge modeling for transient simulations follows that in [2] closely. The resulting charge-based model [3] is much more than a simple equivalent circuit. The model algorithm, implemented in SOISPICE-2, involves iterative, Newton-like numerical solutions of the implicit system of model equations. There are two main iteration loops in the algorithm, required for the derivations of V_{LDS} and V_{LDD} coupled to the channel analysis. SOISPICE-2 is structured to allow user options in the model. For example, the BJT can be turned off by specifying a device-line parameter, and the LDD or LDS region can be eliminated by specifying a length parameter as zero on the model line.

SOISPICE-2 has been supported by numerical device simulations using PISCES [3]. For example, the SOISPICE-2-simulated current-voltage characteristics of a fully depleted SOI MOSFET with a 0.5-μm channel length in a 100-nm-thick film shown in Figs. 2 and 3 are consistent with those predicted by corresponding PISCES simulations. The predicted benefits of an LDD and LDS, doped in this example at 10^{17} cm^{-3}, in controlling the BJT-induced on-state breakdown (Fig. 2) and off-state latch (Fig. 3) of the device are apparent. In all cases of BJT activation, the positive feedback triggered by generated hole injection into the body, which raises V_{BS}, and the subsequent enhancement of the impact ionization by the BJT current becomes regenerative when $\beta(M-1) \simeq 1$. The LDD and the LDS are both effective in controlling this activation by limiting (M-1) and β respectively [3], [4], but, as evident in Fig. 2, at the expense of reduced drive current because of V_{LDS} and V_{LDD}. Referring to Fig. 3, we note that SOISPICE-2 does not predict the "snapback" in the off-state latch characteristics

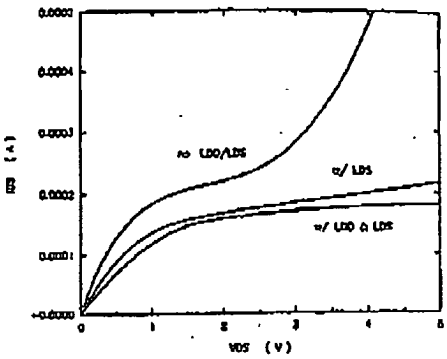

Fig. 2. Simulated on-state breakdown characteristics of SOI MOSFETs with and without LDD/LDS at (V_{GS}-V_T) = 2V.

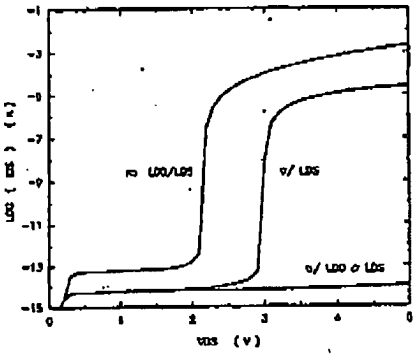

Fig. 3. Simulated off-state latch characteristics of SOI MOSFETs with and without LDD/LDS at V_{GS} = -3V.

[4]. This phenomenon can occur in actual devices, probably when additional components of I_R, which affect $\beta(V_{BS})$, obtain because the devices are not fully depleted in the off state. The utility of SOISPICE-2 is not restricted however because reliable design optimization should be based on the holding voltage (in Fig. 3) and not on the actual latch voltage (which is higher).

SOI CIRCUIT SIMULATIONS

To rigorously assess the viability of SOI CMOS VLSI, the effects of the floating body and the parasitic BJT as induced by actual circuit operation must be studied. Interesting results are obtained from SOISPICE-2 digital circuit simulations. Consider initially the simple SOI CMOS inverter. It is obvious that in the output-high steady state, if V_{DD} is greater than the off-state latch voltage, the n-channel transistor will latch, causing excessive standby current. The high-state voltage is thus lowered and, depending on the conductance of the p-channel transistor, the inverter can lose functionality if the holding voltage is extremely low. Such failure is indeed a tendency in deep-submicron devices as implied by (3) and (4). This condition can also be induced by the pull-up transient if V_{DD} is greater than the holding voltage demonstrated in Fig. 3. In Fig. 4, simulated transient switching characteristics of an SOI CMOS inverter are shown. The inverter comprises 0.5-μm n- and p-channel transistors with fully depleted, floating bodies in 100-nm films. Note the transient latch, and the beneficial effects of the LDD and LDS on the inverter output-voltage swing and supply-voltage current in Fig. 4. Without the LDD/LDS, the n-channel MOSFET latches during the

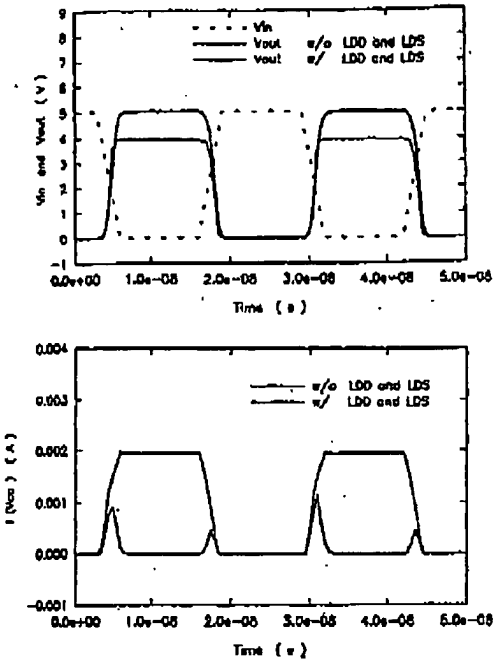

Fig. 4. Simulated SOI CMOS inverter switching transients (output voltages and supply-voltage currents) for devices with and without LDD/LDS.

pull-up transient, resulting in significant standby current and reduced high-state voltage. In this case, the parasitic BJT in the n-channel device is triggered by transient channel current-induced impact ionization. Note that this transient latch will be governed by the fall time of the input voltage pulse; a shorter time tends to prevent the latch by removing the channel current prior to significant increase in V_{DS}. The off-state latch however can be triggered by other (i.e., leakage) currents in the MOSFET structure, so the standby-current problem is pervasive if V_{DD} exceeds the latch voltage of the n-channel transistor. (We are neglecting the possibility of BJT activation in the p-channel transistor.)

During the pull-down transient of the SOI CMOS inverter, the n-channel transistor can latch provided the rise time of the input voltage pulse is sufficiently short. In this case, channel current is quickly turned on, producing enough impact ionization when the output voltage is still high to activate the parasitic BJT. This on-state latch tends to reduce the pull-down delay because of the supplemental BJT current which facilitates discharging of the load. The latch is not sustained in the steady state because V_{DS} is pulled down to zero, precluding any continued impact ionization. SOISPICE-2 simulations of this transient, for varying fan-out (or load capacitance) with and without the BJT activation, reveal however that the speed benefit is only modest. In Fig. 5, predicted pull-down delays are plotted versus the fan-out. The n-channel and p-channel gate areas used in the simulations are 0.5 x 5.0 μm^2 and 0.5 x 10.0 μm^2 respectively. The BJT-produced speed-up is less than 25% even for high fan-out. The benefit is minimal mainly because the transient V_{DS} on the MOSFET during the pull-down quickly drops below the (V_{GS}-dependent) holding voltage, thereby deactivating the BJT for most of the transient. The predicted $I_{DS}(t)$ characteristics, with and without the BJT effect, confirm

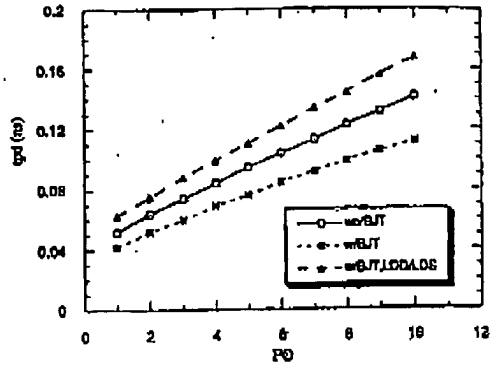

Fig. 5. SOISPICE-2-predicted pull-down delays of SOI CMOS inverter versus fan-out (FO = 1 is equivalent to a 0.0094-pF load), with and without parasitic BJT activation, and with and without LDD/LDS to inhibit the BJT.

this explanation. Thus the standby-current problem appears to be the predominant issue in design optimization. Also included in Fig. 5 are the corresponding delays predicted when the LDD and LDS, both doped at 3×10^{17} cm^{-3} and of length 0.2 μm, are used to inhibit the BJT. Note that these delays are somewhat longer because of the LDD/LDS voltage drops, indicating a critical, but seemingly doable design tradeoff. The delays predicted by SOISPICE-2, even with suboptimal LDD/LDS as in Fig. 5, are substantially shorter than those of the bulk-silicon CMOS counterpart near the L = 0.5 μm scaling level [5].

Consider now the basic six-transistor SOI CMOS SRAM cell shown in Fig. 6, in which the aforementioned effects as well as other unique transient effects can occur due to the floating, fully depleted body. In steady states, the off-state latch can obtain in any of the four n-channel transistors, producing prohibitive standby current in the memory element and/or in the access lines. Furthermore, transient-induced latches and upsets can occur because of the BJT, producing some speed-up as well as standby currents. Consider a write operation, for example writing a "1" (on the drain of N1). The pertinent node-voltage and current transients, obtained from SOISPICE-2 simulations with the parasitic BJT activations, are plotted in Fig. 7. The transistor gate areas used in the simulations are representative of an advanced SOI CMOS technology with L = 0.5 μm. Prior to the gate activation of the access transistors, the high logic level (on the drain of N2) is reduced because of the off-state latch of N2. The initial transient then results in the latching of the access transistors N5 and N6, tending to speed-up the write operation. As for the inverter, this speed enhancement is modest; the write-"1" delay in Fig. 7 is 0.23 ns, which is only about 25% less than the delay predicted

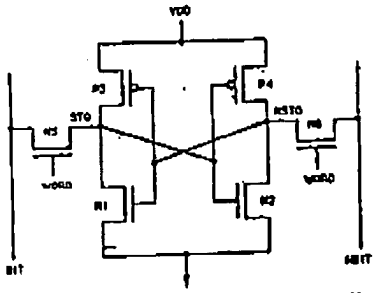

Fig. 6. (SOI) CMOS SRAM cell.

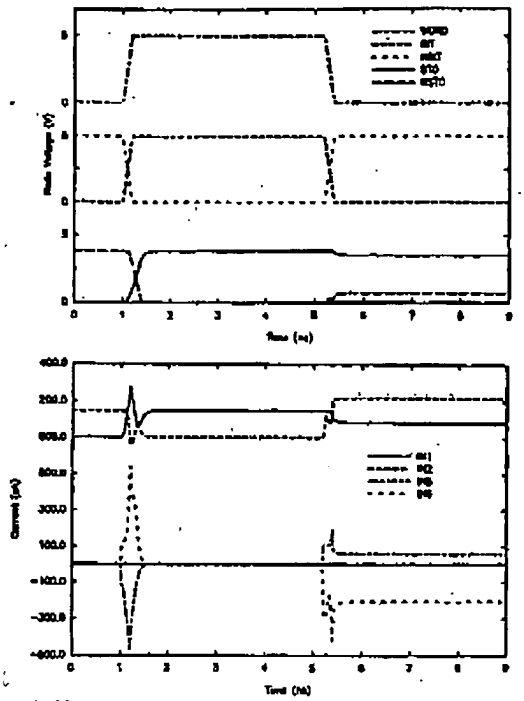

Fig. 7. Node-voltage and current transients from SOISPICE-2 simulation of write-"1" operation in SOI CMOS SRAM cell with BJT activations.

when the BJTs are not activated. When the "1" is written, N5 and N6 are no longer latched, but N1 is latched, keeping the logic level below V_{DD} because of the standby current. If the conductivity of the p-channel load transistors is too low and the holding voltage of the n-channel drive transistors is only a small fraction of V_{DD}, it is impossible to write a logic "1" in the cell. The deactivation pulses finally cause the access transistors N5 and N6 to latch again, resulting in further distortion of the logic levels because of standby current flowing in all the transistors. Clearly the BJT-induced standby currents in the cell are prohibitive, whereas the speed benefit is not significant.

The effects occurring in a read operation are somewhat different. Consider first reading a "0" (on the drain of N1) with the bit lines capacitively precharged (to V_{DD}). Prior to the gate activation of the access transistors N5 and N6, N5 can be latched, thereby enabling the discharging of the precharge capacitor on the bit line. This is illustrated in Fig. 8, which shows SOISPICE-2 simulation results with and without the BJT activations. Note that with the BJTs, the precharge on the bit line coupled to the drain of N1 (and realistically to other storage nodes in the memory array) drops, approaching the holding voltage of N5. Nonetheless the read-"0" operation is done properly, and apparently much faster than without the BJT effects. This speed enhancement is however only an artifact of the BJT-induced source-drain coupling in N5. Consider now reading a "1" in an adjacent cell, with the reduced precharge on the bit lines. The SOISPICE-2 simulation results of this operation show that the net result of the BJT activations in this case is an added delay of the access at best and a general inability to unequivocally read the "1" at worst. This disabling is prohibitive, whereas the apparent speed benefit provided by the BJT to the read-"0" operation is inconsequential.

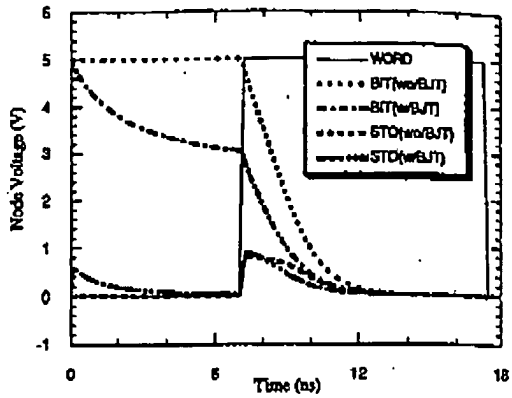

Fig. 8. Node-voltage transients from SOISPICE-2 simulations of read-"0" operation in SOI CMOS SRAM cell with and without BJT activations.

SUMMARY

SOISPICE-2, a version of SPICE2 enhanced with a physical model for the fully depleted SOI MOSFET, was described and used to assess the viability of SOI for submicron CMOS digital circuit applications. Representative circuit (and device) simulations revealed prohibitive standby-current and possible erroneous-function problems caused by activation of the parasitic BJT in the n-channel device structure. The possible benefits, i.e., enhanced speed, afforded by the supplemental BJT current were found to be only modest, and rendered inconsequential by the overwhelming standby-current problems in actual circuit environments. The BJT effects must be constrained to render a viable technology. SOISPICE-2 simulations suggested that an optimally designed LDD/LDS device structure could effect a good tradeoff between alleviating the BJT problems and reducing drive-current capability. The design would require an LDS with low enough doping density to effectively remove (recombine) the holes injected into the body of the n-channel MOSFET. To keep the LDS conductivity acceptably high though, a salicide contact, penetrating the entire SOI film to the underlying oxide and separated from the n-type LDS by a narrow n^+ region, is probably needed [3]. This design tradeoff for viable SOI CMOS VLSI seems doable, partly because of the enhanced drive (saturation) current inherent in the fully depleted SOI MOSFET [6].

ACKNOWLEDGMENT

This work was supported by the U.S. Defense Nuclear Agency and by Texas Instruments, Inc., Dallas, TX.

REFERENCES

1. J.-P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI. Boston: Kluwer, 1991.
2. S. Veeraraghavan and J. G. Fossum, IEEE Trans. Electron Devices, vol. 35, pp. 1866-1875, Nov. 1988.
3. J. Y. Choi, Ph.D. Dissertation, University of Florida, Gainesville, FL, 1991.
4. J.-Y. Choi and J. G. Fossum, IEEE Trans. Electron Devices, vol. 38, pp. 1384-1391, June 1991.
5. T. Yamaguchi and T. H. Yuzuriha, IEEE Trans. Electron Devices, vol. 36, pp. 890-896, May 1989.
6. J. G. Fossum, J.-Y. Choi, and R. Sundaresan, IEEE Trans. Electron Devices, vol. 37, pp. 724-729, March 1990.

Technology Trends of Silicon-On-Insulator - Its Advantages and Problems to be Solved -

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Abstract

Recent progress in SOI technology is reviewed and problems which need be solved are discussed. Emphasis is placed on the substrate floating effect, for which the bandgap engineering method is proposed for the first time. It is demonstrated that Si-Ge formation in the source region can improve the drain breakdown voltage significantly.

1. Introduction

SOI is gaining recognition as a solution for low-power, high-speed, and low-cost ULSIs which are essential for next-generation, multimedia computer systems. With this background, SOI technology has made rapid and substantial progress in the past several years. Especially, outstanding progress in substrate technology has enabled device/process engineers to make access to SOI substrates easier than ever before.

This paper reviews the advantages of SOI and discusses what problems need to be overcome to make it a practical technology. For the substrate floating effect, a bandgap engineering using a Si-Ge source structure is proposed.

2. Advantages of SOI for next-generation ULSIs

From a number of experiments, it has been established that SOI-CMOS operates at a high speed under a low voltage [1-3]. Application to low-voltage logic LSIs may be quite attractive as the nearest target for SOI technology, in that the cost burden for SOI substrates in the early stage can be efficiently absorbed because of the relatively high chip price.

Application to high-density DRAMs, such as 256M or 1G bit DRAMs, is also becoming very attractive because of the soft-error hardness which enables construction of a memory cell in a simple manner. The soft-error hardness has been experimentally demonstrated using a 0.5 μ m rule DRAM cell [4]. We have investigated if soft-error hardness still holds true for 0.15 μm rule DRAM cells by using 3D simulation. Results showed that, although the substrate floating effect can cause a leakage current which enhances the charge collection (Fig.1), the total collected charge at the diffusion region is approximately one-order-of-magnitude smaller than the critical value for soft-error occurrence in bulk Si. It can be also seen that a simple relation holds between a collected charge, Q_{coll}, and the initially-generated charge, Q_{init}, i.e., Q_{coll} does not exceed $h_{FE} \times Q_{init}$ (Fig.2). Since chip-cost counts more in DRAM applications than in other applications, low-cost process design, as well as stable wafer supply will be crucial.

3. Problems to be solved

Among various problems in SOI technology (Table 1), the substrate floating effect may be the most fundamental and the toughest. This effect appears as a low drain breakdown voltage [5], the kink effect [6], or current instability in switching operation [7]. Although reduction of a supply voltage seems to alleviate the low drain breakdown, this problem will remain in the next generation because the breakdown voltage decreases with decreasing a channel length. To deal with this problem, various methods have been proposed. However, every method is subject to disadvantage to a lesser or greater degree (Table 2). For example, the body-contact scheme which seems to provide the most effective method except for area penalty suffers from a decrease in breakdown voltage with an increase in a channel width (Fig.3).

4. Concept of the bandgap engineering method

It is known that the substrate floating effect is caused by hole accumulation in the channel region. The bandgap engineering method aims at narrowing the bandgap at the source, thereby enhancing hole flow toward the source. Suppose the valence band at the source is uniformly shifted upward by δE_g, then hole current will be increased in an exponential manner as $exp(\delta E_g / k_B T)$. If δE_g is 0.12 eV, current enhancement will be 100 times as high. Note that the bandgap narrowing at the source exponentially

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increases the intrinsic carrier density n_i, which in turn increases the hole density in thermal equilibrium. That is, the bandgap narrowing at the source is equivalent to drastically enhancing the "conductance" of the hole flow in the source region. As a quick check, the effect of the bandgap narrowing was studied by simulation in which the bandgap narrowing due to the so-called heavy doping effect [8,9] was switched on and off. Results supported above consideration. However, the bandgap narrowing due to heavy doping is already implemented in actual devices. The most practical way to further decrease the energy bandgap will be to form a Si_xGe_{1-x} region in the source (Fig.4). An implantation of Ge would be the most practical way to achieve that structure. In this case, the Si-Ge region will be formed "inside" the PN junction between the source and the channel region. As a result, holes will sense an energy barrier near the source region in the same way as in the case where there is no Si-Ge region. Still, hole current enhancement by Si-Ge formation is expected to occur, because a Si-Ge region will work to enhance hole diffusion because of its enhanced hole-conductance as described above.

We will show below that 1) the expected improvement effect does occur, 2) the bandgap of Si can be decreased by Ge implantation, 3) with a practical range in Ge dosage.

5. Experiments

Germanium was implanted with the acceleration voltage of 50 kV and a dosage of $1 \times 10^{16} cm^{-2}$ onto the source and drain regions after post-oxidation in 0.15 μm gate length Nch SOI-MOSFETs. Thermal annealing was carried out at 850°C after As implantation for N^+ regions. SIMS measurement showed that Ge concentration exhibited $5 \times 10^{21} cm^{-3}$ (10 % of Si) at the maximum. Comparison of IV characteristics of a conventional and Ge-implanted device (Fig.5) shows that the drain breakdown voltage in a low gate bias region is improved by as much as 1 V, by Ge implantation. Note also that the breakdown voltage in a high gate bias region is improved as well, by approximately 0.5 V. I_d vs.V_d characteristics in the low current region (Fig.6) show that the latch voltage is improved by 1.1 V for the gate bias of $V_{gt} = -1$ V by Ge implantation. These results indicate that Ge implantation effectively suppresses a parasitic bipolar action. RBS measurement revealed that almost all of the implanted Ge atoms are located at substitutional sites. TEM observation also supported this, i.e., the crystal in the source region was epitaxially regrown and few defects were found. From these results, it was considered that valence electrons in Ge atoms might have formed some "well-defined" valence band with valence electrons in Si. To study how the bandgap of silicon was changed by Ge implantation, a photo-electronic emission experiment was conducted. If the valence band edge shifts upward, then the threshold energy at which photo-electronic emission is initiated (the work function) should be decreased. Results showed that the work function did exhibit a decrease with an increase of Ge dosage (Fig.7). From this results, it was estimated that the valence band shift is approximately 0.1 eV for $1 \times 10^{16} cm^{-2}$ Ge dosage. To study whether the observed improvement in the drain breakdown voltage was reasonably explained by the bandgap narrowing effect, device simulation was carried out by implementing physical parameters concerning Si-Ge. The simulation revealed that the improvement in the drain breakdown voltage amounted to approximately 1 V, which agreed well with the experiment (Fig.8). It is now clear that Ge implantation into the source provides quite a practical and effective method in that there is no disadvantage as was seen in conventional methods (Table 2).

6. Conclusions

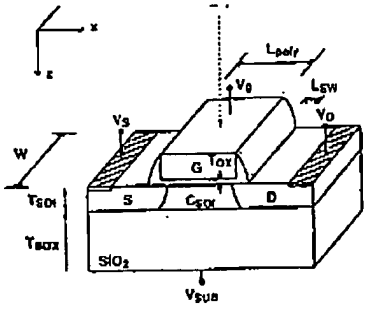
Recent developments and problems in SOI technology have been described. For the substrate floating effect, a novel countermeasure has been presented. After so many breakthroughs and experiments, SOI technology has made remarkable progress in a short time. To date, developments in fields ranging from device/process, circuit, device physics, and substrate technology have come to affect each other, constituting an effective positive feedback loop. If this feedback is maintained, the development of SOI will be further accelerated and it will not be long before SOI will be used as quite as conventional a technology as bulk silicon technology has so far been.

[Acknowledgments]

The authors wish to thank Mr.Y.Nakashima of Riken Keiki Corp., for his collaboration in the experiment. They are also grateful to Dr.K.Yamada of the Toshiba R & D Center as well as to Prof. Y.Shiraki of the University of Tokyo for having precious discussions on Si-Ge. They also thank Dr.T.Arikado and Dr.H.Hara of the ULSI Research Labs for their encouragement throughout this work.

[References]

[1] Y.Yamaguchi et al.; IEEE, vol.ED-40, No.1, 1993, p.179.
[2] G.G.Shahidi et al.; Ext. Abst. of the 1994 Int. Conf. on SSDM, Yokohama, 1994, p.265.
[3] B-Y.Huang et al.; Ext. Abst. of the 1994 Int. Conf. on SSDM, Yokohama, 1994, p.268.
[4] K.Suma et al.; Tech. Abst. of ISSCC 94, 1994, p.138.
[5] M.Yoshimi et al.; IEEE, vol.ED-37, no.9, 1990, p.2015.
[6] K.Kato et al.; IEEE, vol.ED-32, no.2, 1985, p.458.
[7] K.Kato et al.; IEEE, vol.ED-33, 1986, p.133.
[8] J.W.Slotboom et al.;Sol.St.Elect., vol.19, 1976, p.857.
[9] N.Shigyo et al.;IEICE Trans. Electron., vol.E75-C, 1992, p.156.



$L_{poly} = W = 0.15\mu m$, $L_{SW} = 25nm$
$T_{ox} = 6nm$, $C_{SOI} = 5\times10^{15}cm^{-3}$, p-type
$T_{SOI} = 40nm$, Source/Drain $= 1\times10^{18}cm^{-3}$, N^+
$T_{BOX} = 100nm$, $x_j = 40nm$
$V_S = V_{SUB} = 0V$

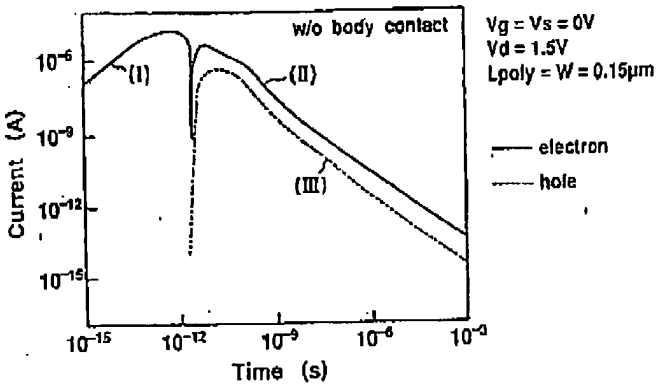
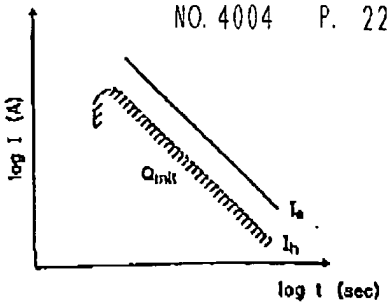


Fig.1 Simulation result of a source current (bottom) after an 5 MeV alpha-particle hits the channel of a 0.15 μm gate length Nch SOI MOSFET (top). The current (I) is due to initially generated electrons which flow out to the source in psec order. The current (II) is due to leakage electrons which flow from the source to the drain for a long time period. The current (III) is due to holes which are the origin of the leakage current (II). The collected charge after 1 sec is 2.6 fC.

Problems

- Device — Substrate floating effect (V_{BD} decrease, Kink)
  - V_D adjustment
- Process
  - Isolation
  - Low parasitic resistance (Silicide, Elevated S/D)
  - Gate material
  - Oxide reliability
- Circuit — Design optimization
- SOI substrates
  - Quality (ΔT_{SOI}, Defects)
  - Cost (~Epi wafer)
  - Stable supply

Table 1 Problems to be solved in SOI technology



$$I_e(t) = h_{FE} \cdot I_h(t)$$

$$Q_{coll}(T) = \int_0^T I_e(t)\,dt$$

$$= \int_0^T h_{FE} \cdot I_h(t)\,dt$$

$$\leq h_{FE} \int_0^\infty I_h(t)\,dt$$

$$= h_{FE} \cdot Q_{init}$$

$$\therefore\ Q_{coll}(T) \leq h_{FE} \cdot Q_{init}$$

Fig.2 Schematic diagram for the time-dependence o. the leakage electron current and the hole current shown in Fig.1. The leakage current flows via parasitic bipola action due to the substrate floating effect. It follows tha the maximum collected charge due to the leakage will no exceed the value $h_{FE} \times Q_{init}$, where h_{FE} is the curren gain of the parasitic bipolar device and Q_{init} is the hole initially generated by the hit event.

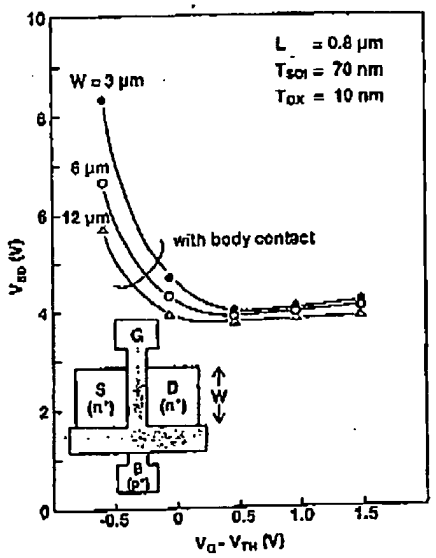


Fig.3 Measured drain breakdown voltage (V_{BD}) of Nch SOI MOSFETs having body contacts as a function of gate voltage. The channel width (W) is a parameter. V_{BD} in the low gate bias region tends to decrease significantly with increasing the channel width.

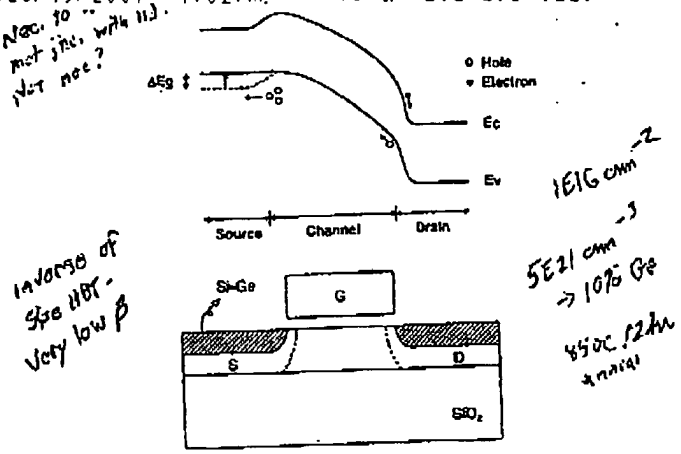


Fig.4 Schematic diagram of the bandgap engineering method (top). Practically, a Si-Ge layer is formed by implantation in the source region, which also works to promote the hole flow toward the source region (bottom).

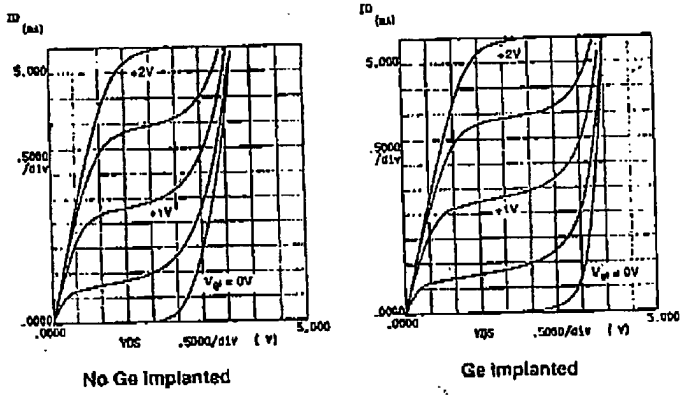


Fig.5 Comparison of I_d versus V_d between a conventional SOI-MOSFET and a Ge-implanted SOI-MOSFET. It should be noted that the drain breakdown voltage has improved by as much as 1.0 V and 0.5 V for a low and a high gate bias region, respectively.

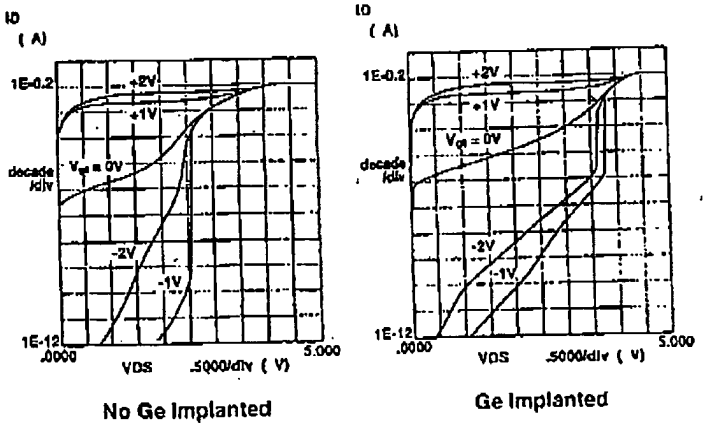


Fig.6 Comparison of I_d versus V_d between a conventional SOI-MOSFET and a Ge-implanted SOI-MOSFET in a low drain current region. It should be noted that the latch voltage exhibited a significant increase. For $V_{g1} = -1$ V, the latch voltage improved by as much as 1.1 V due to Ge implantation.

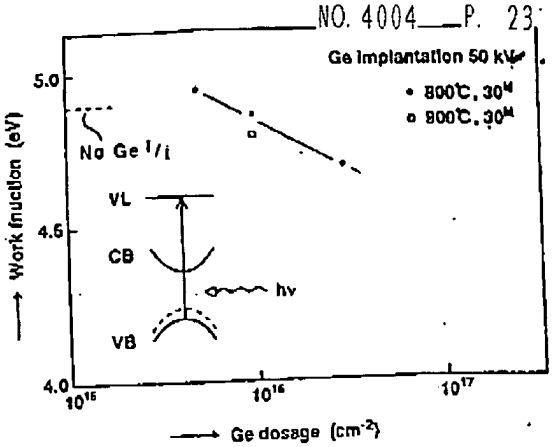


Fig.7 Dependence of work function of Ge-implanted SOI film on Ge dosage. The work function was defined by the threshold energy of photo-electronic emission spectra. A decrease in the work function reflects an upward shift of the valence band.

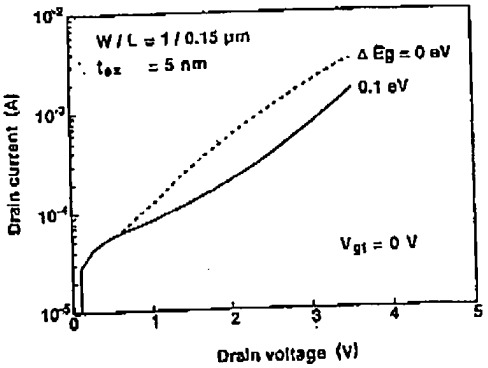


Fig.8 Simulated I_d versus V_d relation taking into account Si-Ge region formation in the source region. Note that the assumption of 0.1 eV decrease in the bandgap reproduced approximately 1.0 V increase in the drain breakdown voltage, which agrees well with the experiment shown in Figs.5 and 6.

Method \ Drawbacks	Area penalty	Id degradation	W dependence	Process complexity	S/D irreversibility
LDD	No	Yes	No	No	No
Body contact	Yes	No	Yes	No	No
Source-tie	No	Yes	Possible	No	Yes
Lifetime killer	No	Yes	No	No	No
Field shield	No	No	Possible	Possible	No
Bandgap engineering	No	No	No	No	No

Table 2 Comparison of countermeasures for the substrate floating effect. Every conventional method has some disadvantage. W dependence for the body contact method is shown in Fig.3. In contrast, the bandgap engineering method has no such demerits.

(7)

BODY CHARGE RELATED TRANSIENT EFFECTS IN FLOATING BODY SOI NMOSFET's

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Abstract

The transient operation of submicrometer floating body SOI NMOSFET's is studied and measured down to a nanosecond time scale. We emphasize the role of the overall hole charge in the body of the device, for a global understanding of the transient phenomena: drain current overshoot or undershoot, memory effect, dynamic instabilities... This charge integrates the device history, with a strongly bias dependent time constant, and influences the drain current, mainly by electrostatic action. The resulting transient current instability has to be considered to avoid anomalous circuit operation.

Introduction

There have been several studies examining the transient operation of SOI devices. They showed that the propagation delay may be dependent on frequency [1] and that a drain current overshoot can exist at low drain voltage [2]. Recently, SOISPICE simulations have shown the possible existence of dynamic floating body instabilities in partially depleted SOI devices [3], but, up to now, no experimental data are available in the literature for submicrometer devices. In this work, we report transient measurements on a nanosecond scale in floating body SOI NMOSFET's, and transient effects analysis by 2-D numerical simulation with hydrodynamic equations. In addition, this work is a comprehensive study of the transient effects in SOI devices, leading to a general explanation based on the overall majority carrier charge in the body of the device.

Measurements and simulations

The devices used in this study were partially depleted SOI NMOSFET's fabricated on conventional SIMOX material. The silicon film thickness, t_{Si}, gate oxide thickness, t_{ox1}, and buried oxide thickness, t_{ox2}, are 75nm, 5nm and 380nm respectively. For an effective channel length of 0.15µm, the low V_D threshold voltage has been adjusted to 0.5V by ion implantation.

To get the transient drain current on a nanosecond time scale, we used the measurement set-up shown in Fig. 1, [4]. The gate is continuously pulsed, between a low level, V_{GL}, and a high level, V_{GH}, with a rise/fall time of 1ns, whereas the drain voltage is monitored on a sampling oscilloscope, through a 50 Ω coaxial load line. The drop of voltage on this load gives the drain current.

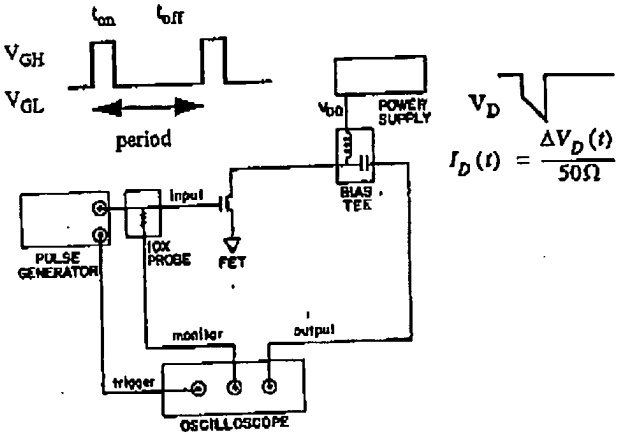

Fig. 1. Measurement set-up for short pulse measurement. The gate is pulsed between a low level V_{GL} to a high level V_{GH}. The drop of voltage in the coaxial 50Ω load is used to get the drain current and is taken into account to get the actual drain voltage.

Fig. 2 shows experimental transient current measured at a gate voltage close to the threshold, on a 0.15µm effective channel length partially depleted NMOSFET's with LDD. After the first 1ns, which corresponds to the gate rise time, there is a drain current transient resulting from the floating body operation, [5]. The strong drain current rise time dependence on the drain voltage is due to the influence of the drain voltage on the impact ionization current: the higher V_D, the higher the impact ionization current and the faster the body steady state is achieved.

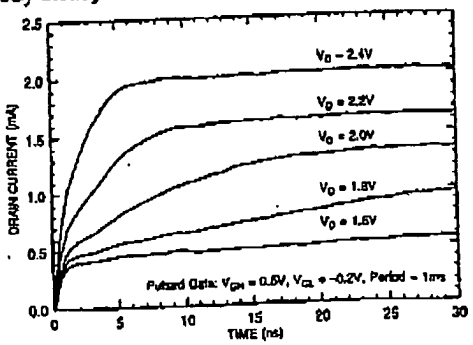

Fig. 2. Drain current transients measured on a partially depleted N-MOSFET: W=25µm, L_{eff}=0.15µm, t_{ox1}=5nm, t_{Si}= 75nm, t_{ox2}=380nm. The width of the gate pulses(-0.2V to 0.5V) is 35ns. The period is 1ms. V_D is varied.

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Simulations with FIELDAY II [6], on a similar device, are in agreement with these measurements,(Fig.3). Increasing V_{GH} to 1V reduces the drain current rise time, but it is still in the ns range.

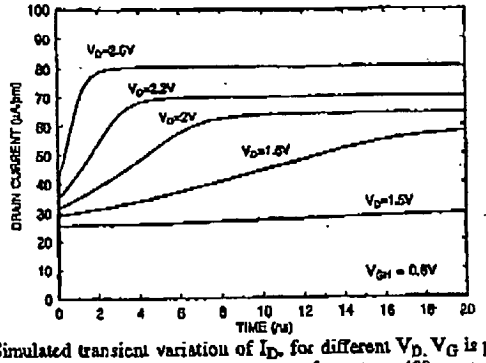

Fig. 3. Simulated transient variation of I_D, for different V_D. V_G is pulsed in 60ps, V_{GL}=0V, V_{GH}=0.6V. L_g=0.2μm, t_{ox1}=5nm, t_{ox2}=400nm, t_{si}=100nm, N_A=6.x10^{17}cm^{-3}.

The gate pulse measurement technique is then used to get the complete $I_D(V_D)$ characteristics at different time delays after the gate voltage rising. Experiments and 2-D simulations on similar device are shown Fig.4 and 5 respectively. There is a clear kink dependence on the timing, such that a circuit performance dependence on timing is expected. At high V_D and for V_G<1V, the drain current is increasing with the delay after

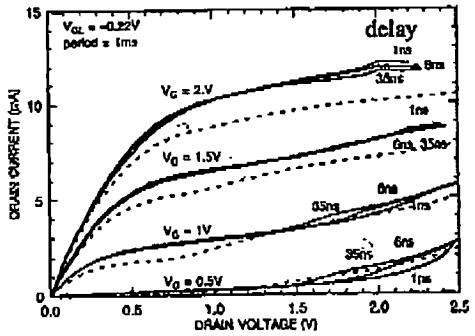

Fig. 4. Measured static (dashed lines) and transient (solid lines) I-V characteristics of a 25μm wide N-MOSFET. I_D is measured at different delays after each gate pulse. Gate pulses of 39ns are applied from V_{GL}=-0.2V. The period is 1ms. The drop of current at high V_D and V_G, for increasing delays, is due to the self-heating. L_{eff}=0.15μm, t_{ox1}=5nm, t_{si}= 75nm, t_{ox2}=380nm.

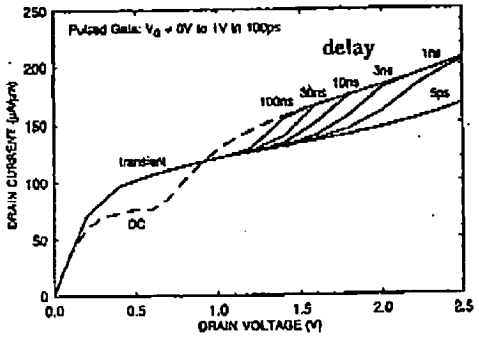

Fig. 5. Simulated static (dashed line) and transient (solid lines) I-V characteristics of a partially depleted N-MOSFET. The current is computed at different delays after the gate rising. L_g=0.2μm, t_{ox1}=5nm, t_{ox2}=400nm, t_{si}=100nm, N_A=6.x10^{17}cm^{-3}. The self-heating is not simulated here.

the gate pulse. Indeed, the kink in transient regime is the closer to the kink in DC as the impact ionization current has sufficient time to charge the body. At low drain voltage, the transient current is higher than the DC current. This overshoot results from a redistribution of the hole charge in the body by capacitive influence of the gate, which induces a forward body biasing and reduces V_T, [2]. At high gate and drain voltages, Fig.4 shows that the transient saturation current is higher than the DC current. This is due to the absence of self-heating a short period of time after the gate voltage rising. In addition, the kink effect is more or less balanced by the gate to body coupling, [7]. 35ns later, a small drop of current, corresponding to the beginning of the self-heating is observed.

Role of the body charge

Because of the global electrical neutrality of the device, there is an electrostatic influence of the overall hole charge in the floating body, Q_h, on the threshold voltage and consequently on I_D. Fig.6 and 7 show the DC variation, vs. V_D and V_G, of this hole charge integrated over the body. A wide range of variation of Q_h is observed, from an absolute minimum, when the gate and the drain contribute to the depletion of the body, to a large value, when the contribution of the impact ionization is maximum. As a general rule, it can be inferred that the transient response of a device is a function of the difference between the final and initial body charges (mainly for the magnitude) and of the hole generation or recombination process (mainly for the time constant).

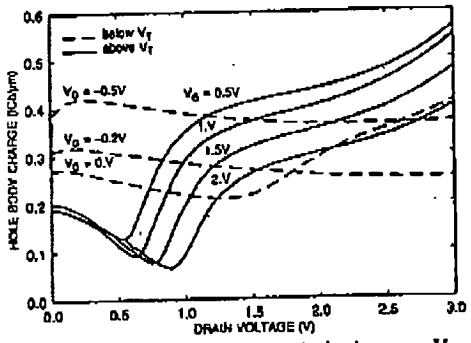

Fig. 6. Simulated DC variation of the hole body charge vs. V_D, for V_G below V_T (dashed lines) or above V_T (solid lines). L_g=0.2μm, t_{ox1}=5nm, t_{ox2}=400nm, t_{si}=100nm, N_A=4.5x10^{17}cm^{-3}.

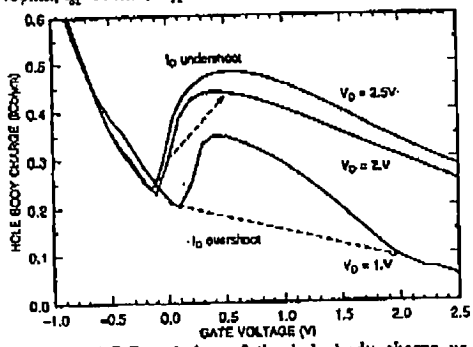

Fig.7. Simulated DC variation of the hole body charge vs. V_G and V_D. L_g=0.2μm, t_{ox1}=5nm, t_{ox2}=.4μm, t_{si}=100nm, N_A=4.5x10^{17}cm^{-3}. The arrows give examples of cases resulting in transient I_D overshoot or undershoot.

For instance, increasing V_G from 0V to 0.5V, for V_D=2V, leads to a transient lack of body charge (Fig. 6), which explains the transient I_D undershoot shown in Fig. 2. On the contrary, increasing V_G from 0V to 1V, for V_D=0.5V, leads to a transient excess of body charge (Fig. 6), which results in the I_D overshoot observed in Fig. 5. Many different cases can be explained in this way.

The real physical variable to characterize the internal state of a floating body device is the overall charge Q_h, not the body voltage. The reason is that Q_h is less sensitive to the external biasing variation during a fast transient (with the exception of a strong body-source forward biasing). On the contrary, V_B is a quasi instantaneous function of this external biasing; its value changes through the capacitive coupling with source, drain, gate and bulk, which induces a hole charge redistribution in the body. This difference of behavior, between Q_h and V_B, is exemplified in Fig. 8, which shows their time variations in a NMOS during a mimic of several switching operations.

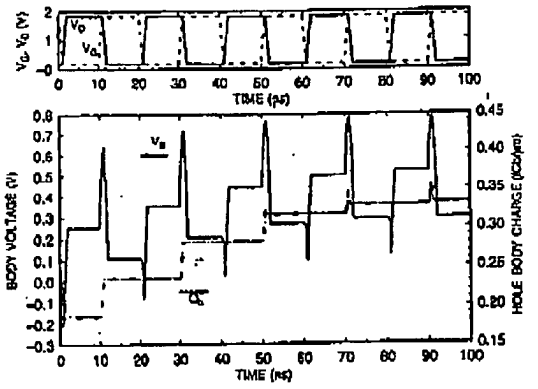

Fig. 8. 2-D simulations of several successive switching of a partially depleted N-MOSFBT. The gate and drain biasing waveforms mimic the real waveforms in a chain of inverters. The body self biasing is plotted in solid line. The integrated hole charge in the body is plotted in dashed line. L_g=0.2µm, t_{ox1}=5nm, t_{ox2}=400nm, t_{si}=100nm, N_A=4.5x10^{17}cm^{-3}. The hole body charge only increases during the "OFF" to "ON" switching, up to the balance with recombination. During all the switching, there is a fast redistribution of the existing hole body charge, resulting in a dynamic change of the body voltage and of V_T.

There is a low initial hole charge in the body, because of the initial DC biasing condition V_D=0V, V_G=2V. Q_h only significantly increases during the short periods of impact ionization current, such that several switching are required to achieve a steady-state regime for which the gain of hole through impact ionization is balanced by the loss through injection in the source and recombination.

Circuits implications

As a first consequence of the previous considerations, for transient operation, the worst case initial condition for drivability (best case for the leakage) is a minimum of Q_h. For our low V_T SOI device, this does not occur at the "OFF" state, V_G=0V and V_D=V_{DD} >1V, when there is a non negligeable impact ionization current induced by the drain leakage current and the strong drain field. In that case, at the "ON" state, V_G=V_{DD} and low V_D, there is a lower amount of hole charge, that does not change for several µs after a device switching from "ON" state to "OFF" state. Consequently, this initial condition must be considered for worst case analysis of "OFF" to "ON" switching of NMOSFET's. It can be approximated by a DC biasing at the "OFF" state, but with a small negative gate voltage instead of V_G=0V (Fig. 7 shows that a minimum of Q_h exists for a lightly negative gate voltage). The role of this low hole charge initial condition is exemplified in Fig. 9, where transient output characteristics have been measured 1ns after fast gate pulses: the lower Q_h case results in a lower I_D. Moreover, in the I_D-V_D curve with V_{GL}=-0.2V and V_{GH}=0.5V, there is a jump in I_D to the V_{GL}=0V curve, at V_D~2.4V. This original feature is correlated to the existence of a switching and hysteresis in the gate voltage characteristics (Fig.10), taking into account the initial drain voltage value, before the drop in the 50Ω load.

For the previous transient I_D measurements, the t_{off}=1ms value between the gate pulses is sufficient to recombine the excess of hole in the body, due to the impact ionization at high V_D. However, using a lower t_{off}, this excess of hole is not fully discharged, which increases Q_h at the beginning of the gate pulses and the measured I_D. We infer that in a real circuit, the drain current will be modulated by the device history.

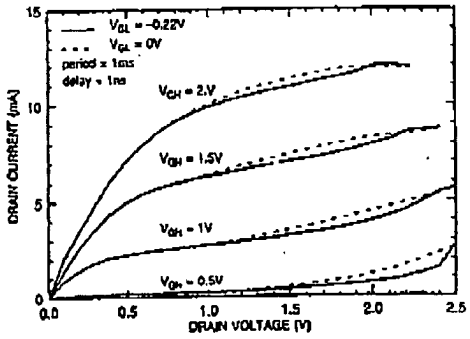

Fig. 9. Transient output characteristics, for conditions minimizing the initial hole body charge, Q_h, at high V_D (solid lines), or for a higher initial Q_h (dashed lines). The current is measured 1µs after the rising of 4ns gate pulses. L_{eff}=0.15µm.

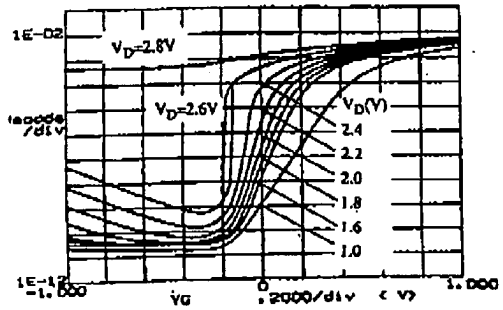

Fig. 10. Measured static subthreshold I-V characteristics of a 25µm wide N-MOSFET. L_{eff}=0.15µm. For V_D=2.6V, there is a switching mechanism which induces an hysteresis cycle.

The influence of this initial body charge on the speed of circuit is studied by the discharge of a capacitive load in a transistor, this simple structure being equivalent to half an inverter. Fig.11 shows the discharge waveforms for different initial conditions. The transient variation of the body voltage (split of quasi fermi potentials) is also represented. As a consequence of the propagation delay dependence on the initial body condition, i.e. on the device history, a jitter could be induced on the signals in SOI circuits. Moreover, the propagation delay being directly related to the saturation current, the sensitivity to the initial body charge can be obtained from the $I_{Dsat}(Q_h)$ curve (Fig.12).

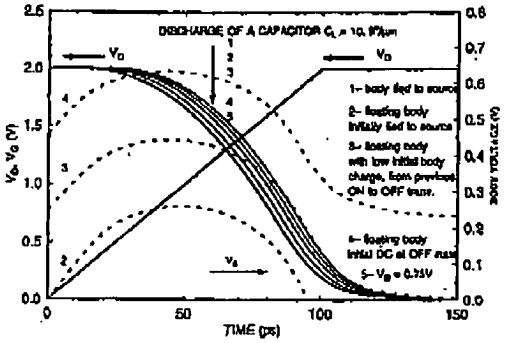

Fig. 11. Simulations of the discharge of a capacitive load by a partially depleted N-MOSFET: drain voltage waveforms (solid lines) and self body biasing (dashed lines) for different initial body conditions. L_g=0.2µm, t_{ox1}=5nm, t_{ox2}=400nm, t_{si}=100nm, N_A=4.5x10^{17}cm^{-3}.

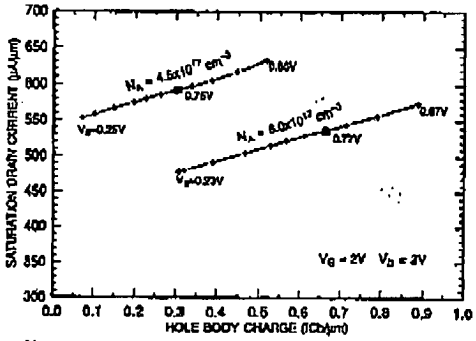

Fig. 12. Simulated variation of the saturation current at V_G=V_D=2V, vs. the hole body precharging, for two different uniform body doping. Squares correspond to DC regimes. L_g=0.2µm, t_{ox1}=5nm, t_{ox2}=400nm, t_{si}=100nm.

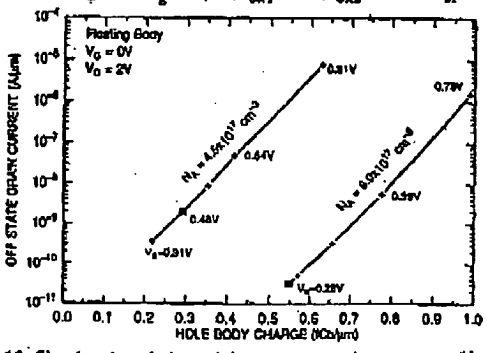

Fig. 13. Simulated variation of the leakage drain current at V_G=0V, V_D=2V, vs. the hole body precharging, for two different uniform body doping. Squares correspond to DC regimes. L_g=0.2µm, t_{ox1}=5nm, t_{ox2}=400nm, t_{si}=100nm.

The influence of the hole body charge on the drain leakage is given in Fig.13.

Taking into account the Q_h dependence on the device history is crucial for the right operation of analog circuits. As an example, we report the observed anomalous operation of a SRAM sense amplifier, which was designed for a bulk technology then used on SOI [5], resulting in a measured transient return to "0" of the output (glitch), when reading two successive "1". After an address transition detection, a pulse is generated to short-circuit the differential inputs (bit lines) of the sense amplifier, in order to speed up the sensing and avoid a race phenomenon during the row and column decoding. Normally, the output of the sense does not change during this operation. However, the change of NMOS biasing in the sense amplifier, results in small I_D overshoot and undershoot which are amplified along the different stages, leading to a glitch on the output. Using body-tied-to-source for the NMOS in the sense removed the glitch, so confirming the previous existence of the floating memory effect.

Summary

In summary, we emphasized and clarified the role of initial and final hole body charges on the transient operation of partially depleted SOI NMOSFET's. 2-D numerical simulations showed that this charge, Q_h, is strongly related to the history of the device, integrating the action of recombination and thermal and impact ionization generation mechanisms. The maximum magnitude of a transient effect, overshoot or undershoot, is directly related to the deviation of Q_h from the initial value to the final value. We also showed that during a transient operation, the body voltage results from a redistribution of the available hole body charge (through gate and drain capacitive coupling to the body), as a function of the instant biasing. In agreement, 2-D simulations and transient measurements, on a nanosecond scale, showed that the drain current time constant is strongly dependent on the device biasing. Further, we gave direct experimental proof of the existence of memory effect in device operation. The dynamic operation of floating body devices is fully explained and must be taken into account for accurate circuit simulation.

Acknowledgments

The authors wish to thank B. Davari and J. Hartmann for management support, G. Fiorenza and S. Furkay for support in using FIELDAYII simulator and R. H. Dennard for many valuable discussions.

References

[1] H. K. Lim and J. Fossum, IEEE Trans. Electron Devices, Vol. ED-31, N0.9, pp. 1251-1258, 1984

[2] K. Kato, and K. Taniguchi, IEEE Trans. Electron Devices, Vol. ED-33, pp. 133-139, 1986

[3] D. Suh and J. Fossum., IEEE IEDM Tech. Dig., pp. 661-664, 1994

[4] K. A Jenkins and J. Y.-C. Sun, IEEE Electron Device Lett., Vol. 16, N0.4, pp.145-147, 1995

[5] C. Lerous, J. Gautier, A.J. Auberton-Herve, B. Giffard and M. Spalanzani, Microelectronic Engineering 15, Amsterdam: Elsevier, pp.199-202, 1991

[6] S. Furkay et al. "FIELDAYII User's Manual, Version N0 7.3.0", IBM Technology Modeling, East Fishkill, Hopewell Junction, NY 12533, 1993.

[7] J. Gautier and J. Sun, "On the transient operation of partially depleted SOI NMOSFET's", Electron Device Lett., Vol.16, N0.11. 1995.

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 42, NO. 4, APRIL 199

A Physical Charge-Based Model for Non-Fully Depleted SOI MOSFET's and Its Use in Assessing Floating-Body Effects in SOI CMOS Circuits

Dongwook Suh and Jerry G. Fossum, *Fellow, IEEE*

Abstract—**A new model for the non-fully depleted (NFD) SOI MOSFET is developed and used to study floating-body effects in SOI CMOS circuits. The charge-based model is physical, yet compact and thus suitable for device/circuit simulation. Verified by numerical device simulations and test-device measurements, and implemented in (SOI)SPICE, it reliably predicts floating-body effects resulting from free-carrier charging in the NFD/SOI MOSFET, including the purportedly beneficial supra-ideal subthreshold slope due to impact ionization and a saturation current enhancement due to thermal generation. SOISPICE CMOS circuit simulations reveal that the former effect is not beneficial and could be detrimental, but the latter effect can be beneficial, especially in low-voltage applications, when accompanied by a dynamic floating-body effect that effectively reduces static power. The dynamic floating-body effects are hysteretic, however, and hence exploitation of the beneficial ones will necessitate device/circuit design scrutiny aided by physical models such as the one presented herein.**

I. Introduction

FULLY depleted (FD) SOI MOSFET's have drawn much attention for CMOS IC applications because of their performance advantages which include enhanced current, ideal subthreshold slope, and reduced short-channel effect [1]. These advantages, over non-fully depleted (NFD) SOI and bulk-Si MOSFET's, tend to fade, however, as the channel length is scaled to deep-submicrometer values; the current enhancement is limited by velocity saturation [2] and the subthreshold slope is degraded by source/drain charge sharing [3], which underlies the short-channel effect. Furthermore, acceptable threshold voltage dictates higher body doping for the FD technology, and thus thinner SOI films, to maintain full depletion of the body, which require tighter control of the material production as well as the device processing. Consequently, there is growing interest in the NFD (or partially depleted) SOI technology in which an acceptable threshold voltage can be readily achieved. Also because of the thicker SOI film, NFD design allows vertical doping engineering [4] and/or halo implantation (DI-LDD) [5], which have been incorporated in scaled bulk technology for control of the short-channel effect.

Manuscript received July 20, 1994; revised November 29, 1994. The review of this paper was arranged by Associate Editor D. A. Antoniadis. This work was supported by Texas Instruments, Inc., and the Semiconductor Research Corporation.

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IEEE Log Number 9409066.

For design in SOI CMOS, there is a tendency to use bulk-Si MOSFET models, empirically modified to apply to the SOI device, be it NFD or FD. The reliability of such models, however, is questionable because of unique SOI effects that can be significant. For example, capacitance associated with the underlying SiO_2 can be important if the oxide is scaled, and floating-body effects due to (dc or transient) free-carrier charging can influence, or even control [6], [7] the device performance. Floating-body effects in the NFD technology are most prevalent because of the dependence of threshold voltage on body voltage (which is insignificant in the FD technology [1]). These effects can be detrimental or beneficial, and hence must be inhibited or should be exploited in optimal design of the NFD technology. However, the device-performance merits do not translate into circuit-performance enhancements in a straightforward manner, and hence the assessment of the floating-body effects must be done comprehensively at the circuit as well as the device levels.

A compact physical model for the NFD/SOI MOSFET is thus needed. In this paper, we present such a model, and use it, implemented in SOISPICE [7], to give insight regarding optimal device/circuit design of the NFD technology. In particular, we show how floating-body effects produce the supra-ideal subthreshold slope and an enhanced saturation current in actual devices and how they can influence dynamic performance and static power in CMOS circuits, and we discuss whether they should be inhibited or exploited in optimal SOI design.

II. Model Formalism

Fig. 1 shows a schematic cross section of a typical (n-channel) NFD/SOI MOSFET with lightly doped drain/source (LDD/LDS) and halo implant. It is a five-terminal device when the body is contacted. Floating body is a model option, as are the LDD/LDS and halo regions. The intrinsic body is assumed to comprise two regions, defined by the vertical doping variation and separated by a high–low junction as indicated. The low-doped region (N_B) is assumed to be fully depleted when the channel is formed while the high-doped region (N_H) is assumed to remain neutral. These model assumptions pertaining to the doping are representative of the body structure that results from vertical doping engineering for control of the short-channel effect and prevention of back-channel turn-on.

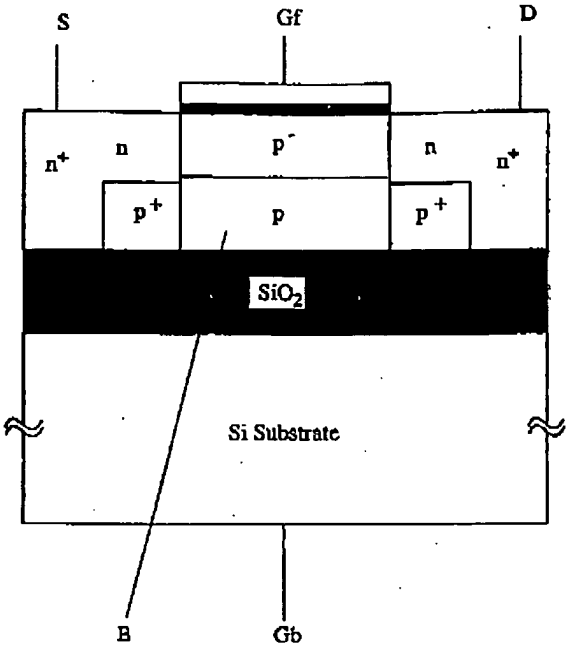

Fig. 1. Representative cross-sectional view of the general NFD/SOI MOSFET structure, including LDD/LDS and halo (p^+ under LDD/LDS) regions.

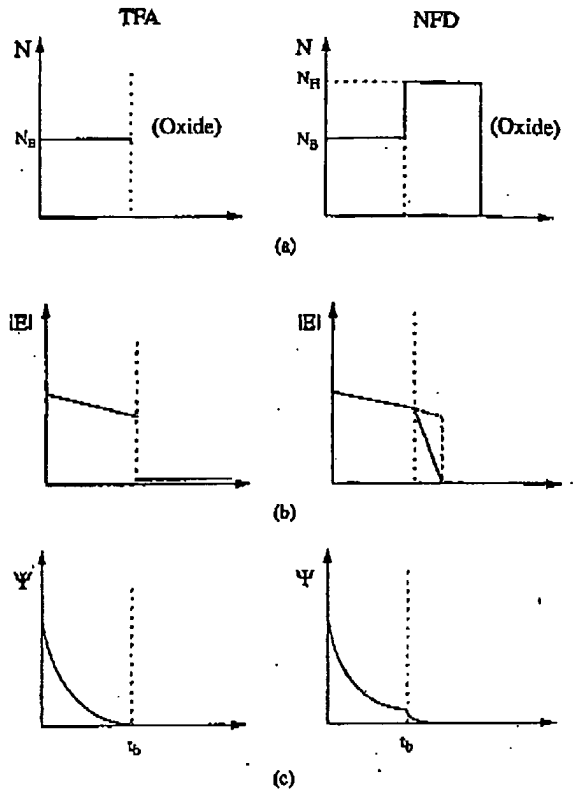

Fig. 2. Comparison between TFA/SOI [8] and NFD/SOI MOSFET's showing similar electrical properties.

The high–low junction in the NFD body effectively confines the depletion region under the front gate, and the underlying quasi-neutral region decouples the back gate electrically. Thus the electrical properties of the channel region in the NFD device mimic the TFA/SOI (thin-film-accumulated) condition [8] in which accumulated holes at the back interface prevent the back gate from electrically interfering with the channel. Fig. 2 illustrates the similarities in electrical properties of the NFD and TFA devices. If the high–low junction were ideal (i.e., infinite N_H), the charge condition in the NFD device would be identical to that of a TFA device, with the back surface potential (Ψ_{sb}) pinned at the body-source voltage V_{BS}. Consistent with the model assumptions, we define an effective film thickness (t_b), which is (approximately) the high–low junction depth or the maximum depletion-region width in strong inversion, and use the TFA formalism [8] as the basis for the NFD model. The TFA short-channel-current (I_{CH}) analysis is expanded to account for weak- and moderate-inversion conditions. To completely characterize the physical properties of the NFD/SOI MOSFET, impact-ionization current (I_{Gi}), parasitic-BJT current (I_T), recombination current (I_R), and thermal-generation current (I_{Gt}) are also included in the model, and terminal charging currents are defined to simulate the charge dynamics. The generation/recombination currents and the body charging current are crucial for proper accounting of the floating-body effects on channel current.

To facilitate the model development, we separately characterize the intrinsic region under the gate and the optional extrinsic regions (LDD/LDS, halo), linking the regional solutions as reflected by the equivalent circuit of Fig. 3. The accounting for the halo region is done by defining an effective (higher) N_B which yields a higher threshold voltage. The LDD/LDS analyses define the voltage drops across the LDD and LDS. The ohmic portion of these drops is simply modeled by a lumped resistance added to the parasitic series resistance in the source and drain, while a possible nonohmic component for the LDD, due to high electric field and concomitant depletion, is accounted for physically. This voltage drop, denoted as V_{LDD} in Fig. 3, is subject to the analysis of the channel. Thus an iterative solution scheme is adopted. The solution defines quasi-static terminal charges, as well as the mentioned currents, which are used to characterize the charging/discharging currents.

A. Channel Current (I_{CH})

The channel current is derived from the characterization of the charges under the front gate. The derivation can be facilitated by considering two distinctive conditions in which either drift or diffusion dominates the conduction mechanism, i.e., by assuming strong or weak inversion. The moderate-inversion characteristics are represented by connecting these two regions via cubic-spline interpolation [9]. The boundaries of the moderate-inversion region are physically defined by the dependence of the channel charge Q_c on the front-gate bias V_{GfS}, following [10]. This dependence is derived by first applying Gauss's law to the front-gate structure for $V_{DS} = 0$ [8]:

$$V_{GfS} = V_{FB} + (1+\alpha)\Psi_{sf0} - \frac{Q_{b(\text{eff})}}{2C_{of}} - \frac{Q_c}{C_{of}} - \alpha V_{BS} \quad (1)$$

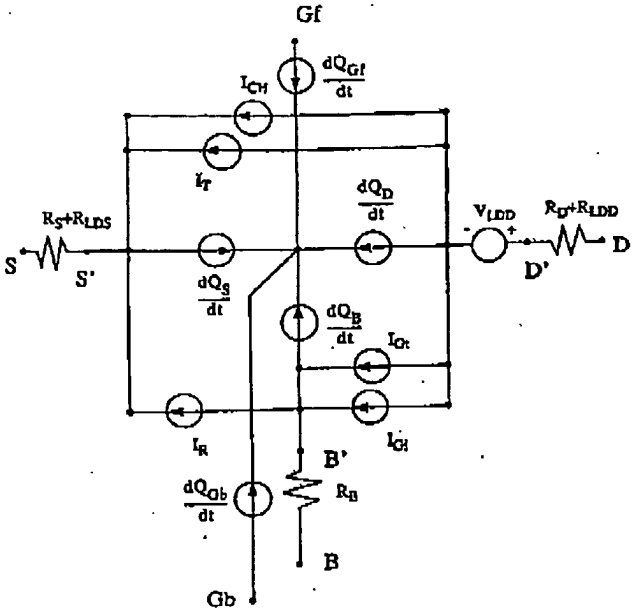

Fig. 3. Network representation of the NFD/SOI MOSFET model.

where Ψ_{sf0} is the surface potential, V_{FB} is the flat-band voltage, C_{of} is the oxide capacitance defined as ϵ_{ox}/t_{of}, and α is C_b/C_{of} where C_b is defined as ϵ_{si}/t_b; $Q_{b(\text{eff})}$ is the depletion charge associated with the front gate, which is set to $Q_b = qN_Bt_b$ is the weak-inversion formalism, but is less than Q_b due to (V_{BS}-dependent) source/drain charge sharing in the strong-inversion analysis.

Differentiating (1) with respect to V_{GfS}, we get

$$\frac{d\Psi_{sf0}}{dV_{GfS}} = \frac{C_{of}}{C_{of}+C_b+C_i}. \tag{2}$$

where $C_i = d|Q_c|/d\Psi_{sf0}$. As noted in [10], the lower boundary of strong inversion is determined by the constancy of $d|Q_c|dV_{GfS}$ and the upper boundary of weak inversion by the constancy of $d(\ln|Q_c|)/dV_{GfS}$. With (2), we can express these derivatives as

$$\frac{d|Q_c|}{dV_{GfS}} = \frac{C_{of}C_i}{C_{of}+C_b+C_i} \tag{3}$$

and

$$\frac{d(\ln|Q_c|)}{dV_{GfS}} = \frac{C_{of}}{C_{of}+C_b+C_i}\left(\frac{C_i}{|Q_c|}\right). \tag{4}$$

In (3) and (4), C_i is the only capacitance that varies with bias. Thus we define the moderate-inversion boundaries as the values of V_{GfS} where $C_i = 10(C_{of}+C_b)$ in (3) and $C_i = (C_{of}+C_b)/100$ in (4), respectively. These conditions can be translated to terms of surface potential and gate bias if we express C_i as [11]

$$C_i = \frac{qn_i^2}{N_B}\frac{1}{E_{xf0}}\exp\left(\frac{\Psi_{sf0}}{V_{TH}}\right) \tag{5}$$

where V_{TH} is the thermal voltage (kT/q) and E_{xf0} is the (transverse) electric field at the surface. In weak inversion, the surface field is defined by the depletion approximation [12]:

$$E_{xf0} \cong \frac{\Psi_{sf0}-V_{BS}}{t_b} - \frac{Q_b}{2\epsilon_s}. \tag{6}$$

In strong inversion, the channel charge affects the field, which is obtained from Poisson's equation,

$$\frac{d^2\Psi_{sf0}}{dx^2} \cong \frac{q}{\epsilon_s}\left[N_B + \frac{n_i^2}{N_B}\exp\left(\frac{\Psi_{sf0}}{V_{TH}}\right)\right]. \tag{7}$$

Integrating (7) over the predominant inversion layer, from $\Psi = \Psi_{sf0}$ to $\Psi = 2\phi_F$, describes the surface field as

$$E_{xf0}^2 \cong E_x^2(2\phi_F) + \frac{2qn_i^2V_{TH}}{\epsilon_sN_B}\exp\left(\frac{\Psi_{sf0}}{V_{TH}}\right) \tag{8}$$

where $E_x(2\phi_F) \cong (2\phi_F - V_{BS})/t_b - Q_{b(\text{eff})}/2\epsilon_s$ [12] and $2\phi_F = V_{TH}\ln(N_B/n_i)$.

Substituting (6) and (8) into (4) and (3), respectively, with the aforementioned criteria, we obtain the ($V_{DS} = 0$) moderate-inversion boundaries as

$$\Psi_{sfW} = V_{TH}\ln\left[\frac{N_BE_{xf0}}{100qn_i^2}(C_{of}+C_b)\right] \tag{9}$$

and

$$\Psi_{sfS} = V_{TH}\ln\left[\frac{10N_BE_{xf0}}{qn_i^2}(C_{of}+C_b)\right] \tag{10}$$

where Ψ_{sfW} is the upper limit of weak inversion and Ψ_{sfS} is the lower limit of strong inversion. Note that E_{xf0} in (6) and (8) is dependent on Ψ_{sf0}; therefore a few iterations are required to calculate Ψ_{sfW} and Ψ_{sfS} in (9) and (10).

Due to DIBL and DICE (drain-induced barrier lowering and charge enhancement) [8] in short-channel devices, the surface potential and the channel charge are modulated by the drain bias, and thus the boundaries that separate strong and weak inversion can also depend on V_{DS}. While DIBL directly increases the surface potential in weak inversion by $\epsilon_s\eta t_b/2C_{of}(1+\alpha)$ where $\eta = 2V_{DS}/L^2$ [8], DICE gives rise to increased channel charge under the gate in strong inversion. These effects result in rigid shifts of the values of V_{GfS} that correspond to (9) and (10). These values, with DIBL and DICE, are defined from (1), (9), and (10):

$$V_{TW} = V_{FB} + (1+\alpha)\Psi_{sfW} - \frac{Q_b}{2C_{of}} - \alpha V_{BS} - \frac{\epsilon_s\eta t_b}{2C_{of}} \tag{11}$$

and

$$V_{TS} = V_{FB} + (1+\alpha)\Psi_{sfS} - \frac{Q_{b(\text{eff})}}{2C_{of}} - \frac{Q_c}{C_{of}} - \alpha V_{BS} - \frac{\epsilon_s\eta t_b}{2C_{of}}. \tag{12}$$

Q_c is neglected in (11) because of weak inversion, and in (12) it is calculated by Gauss's law using (8).

When V_{GfS} is greater than V_{TS}, the channel current is calculated by the strong-inversion model, which closely follows the TFA formalism in [8]. The inversion charge is calculated including the short-channel effects such as DICE and charg

sharing, which relates $Q_{b(\text{eff})}$ to Q_b. Field-dependent mobility and velocity saturation are also included; the mobility degradation is due to not only the transverse field but also the longitudinal field. Channel-length modulation is accounted for by the application of Gauss's law to the two-dimensional high-field region near the drain. This characterization gives a physically defined electric field which is also important for modeling the impact-ionization current.

In weak inversion where $V_{GfS} < V_{TW}$, the channel current is predominantly diffusion [11]:

$$I_{\text{CH}} = WV_{\text{TH}}\overline{\mu}_n \frac{d}{dy} Q_c(y) \tag{13}$$

where $\overline{\mu}_n$ is an average channel mobility subject to mobility degradation in the channel, and

$$-Q_c(y) \cong \frac{qn_i^2 V_{\text{TH}}}{N_B E_{xf}} \exp\left(\frac{\Psi_{sf} - V(y)}{V_{\text{TH}}}\right) \tag{14}$$

where $V(y)$ is the quasi-Fermi level separation at y due to V_{DS}. Integrating (13) along the channel gives the expression for the channel current in terms of $Q_c(y)$ in (14), in which Ψ_{sf} is nearly constant [11]. For short-channel devices, however, the surface potential is modulated along y because of the source and drain junctions in the two-dimensional structure. This modulation is difficult to distinguish from the charge-sharing effect; but it can be effectively modeled as channel-length modulation in weak inversion [13]. Thus we assume that (13) and (14), with constant Ψ_{sf}, are applicable only in a central portion of the channel ($y_s \le y \le L - y_d$), the length ($L_e \cong L - 2y_d$) of which is [13]

$$L_e \cong L - 2l_c \ln\left(\frac{L^2}{2l_c^2}\right) \tag{15}$$

where l_c, defined in [8], is structure-dependent. Now integrating (13) from $y = y_s$ to $y = L - y_d$ yields

$$I_{\text{CH}} \cong \frac{Wqn_i^2\overline{\mu}_n V_{\text{TH}}^2}{L_e N_B E_{xf}} \exp\left(\frac{\Psi_{sf}}{V_{\text{TH}}}\right)\left[1 - \exp\left(-\frac{V(L-y_d)}{V_{\text{TH}}}\right)\right]. \tag{16}$$

The total surface potential in (16) is $\Psi_{sf} = \Psi_{sf0} + \Delta\Psi_{sf}$ where DIBL causes $\Delta\Psi_{sf} = \epsilon_s t_b \eta / 2C_{of}(1+\alpha)$ [8]; Ψ_{sf0} is given by (1) with $Q_c \cong 0$:

$$\Psi_{sf0} = \frac{1}{1+\alpha}\left[V_{GfS} - V_{FB} + \frac{Q_b}{2C_{of}} + \alpha V_{BS}\right]. \tag{17}$$

The transverse field in (16) is defined as $E_{xf} = E_{xf0} + \Delta E_{xf}$ where E_{xf0} is given by (6) and ΔE_{xf}, resulting from DIBL, is expressed as [8]

$$\Delta E_{xf} \simeq -\frac{C_{of}}{\epsilon_s}\Delta\Psi_{sf} = -\frac{\eta t_b}{2(1+\alpha)}. \tag{18}$$

The linking of the strong- and weak-inversion current characterizations is done via cubic-spline interpolation [9] across the moderate-inversion region. The moderate-inversion boundaries defined previously are physical, and hence continuity of the channel current and transconductance is ensured. To define the cubic spline, the current and transconductance at each boundary are calculated from the respective formalisms. The derivative in weak inversion is analytically evaluated, while in strong inversion it is numerically determined. The spline is applied to the logarithm of the current in the moderate-inversion region:

$$\ln(I_{\text{CH}}) = \alpha_0 + \alpha_1(V_{GfS} - V_{TW}) + \alpha_2(V_{GfS} - V_{TW})^2 + \alpha_3(V_{GfS} - V_{TW})^3 \tag{19}$$

where the α's are given in terms of the boundary values of $\ln(I_{\text{CH}})$ and $d\ln(I_{\text{CH}})/dV_{GfS}$.

B. LDD Analysis (V_{LDD})

More rigorous LDD analysis is done when a nonohmic voltage drop, V_{LDD}, develops across the LDD [7]. This drop is calculated based on results of the channel analysis, i.e., the channel current and the maximum electric field. The channel analysis is in turn dependent on this drop via diminished intrinsic drain bias ($V_{DS} \rightarrow V_{DS} - V_{LDD}$). Hence an iterative numerical method is adopted to physically link the two analyses.

C. Impact-Ionization Current (I_{Gi})

Impact-ionization current is characterized by evaluating the multiplication factor, $(M-1)$, in the high-field region near the drain. Only weak impact ionization ($M \cong 1$) is relevant (for example to model the BJT-induced breakdown [14]); thus the characterization is done as a post-processing after the channel analysis. The multiplication factor is calculated by integrating the impact-ionization rate over the high-field region, including the high-field portion of the channel and the LDD:

$$(M-1) = \int_{(L-y_d)}^{L} \alpha_0 \exp\left(-\frac{\beta_0}{|E_y|}\right) dy + \int_{L}^{(L+L_{\text{LDD}})} \alpha_0 \exp\left(-\frac{\beta_0}{|E_y|}\right) dy \tag{20}$$

where α_0 and β_0 are empirical impact-ionization coefficients (constants). The first integral of (20) is evaluated following [8] with y_d defined by channel-length modulation, and the second one is calculated using the electric field from the LDD analysis [7]. Then the total generation current due to impact ionization is given as

$$I_{Gi} \cong (M-1)(I_{\text{CH}} + I_T) \tag{21}$$

where I_T is the BJT current.

D. Parasitic-BJT Transport Current (I_T)

The parasitic (lateral) BJT in the MOSFET structure is modeled to account for the loss of gate control it can cause [14]. The injection condition at the source–body junction in the upper depletion region of the NFD device is like that of the FD device [7], but is different in the underlying neutral region where we assume low-injection conditions. The BJT

transport current is hence modeled as comprising components in both the depleted body and the neutral body:

$$I_T \cong WJ_{D0}\left[\exp\left(\frac{V_{BS}}{2V_{TH}}\right)-1\right] + WJ_{N0}\left[\exp\left(\frac{V_{BS}}{V_{TH}}\right)-1\right] \quad (22)$$

where J_{D0} and J_{N0} are structure-dependent constants that can be evaluated via integral charge-control analyses [11] in the relevant body regions. When there is a halo region (i.e., p^+ region under LDS in Fig. 1), the minority-carrier injection into the neutral region tends to be suppressed due to the higher doping density, and thus the second component in (22) is reduced accordingly.

E. Recombination Current (I_R)

The recombination current in the FD device occurs predominantly in the quasi-neutral source region because of carrier separation due to the transverse field in the body [15]. This is not the case in the NFD device, however, due to the neutral region in the body. Thus the pertinent recombination current associated with the source-body junction is modeled generally as [11]

$$I_R \cong WJ_{R0}\left[\exp\left(\frac{V_{BS}}{mV_{TH}}\right)-1\right]+WJ_{S0}\left[\exp\left(\frac{V_{BS}}{V_{TH}}\right)-1\right] \quad (23)$$

where J_{R0} is a structure-dependent constant dependent on recombination lifetime and m (≥ 1) is a nonideality factor; the second component in (23) represents the source-region recombination, and physically limits V_{BS}.

F. Thermal Generation Current (I_{Gt})

The thermal generation leakage current associated with the drain–body junction is assumed to derive from the depletion region in the body [11]:

$$I_{Gt} \cong \frac{qn_iWt_bL}{\tau_G}\left[1-\exp\left(\frac{V_{BD}}{V_{TH}}\right)\right] \quad (24)$$

where τ_G is the generation lifetime.

G. Charge Modeling

The terminal charges Q_{Gf}, Q_D, and Q_S are described following [8], and Q_{Gb} follows from Gauss's law applied to the back-gate structure. Then charge neutrality of the device defines Q_B:

$$Q_S+Q_D+Q_{Gf}+Q_{Gb}+Q_B+Q_{ff}+Q_{fb}=0 \quad (25)$$

where Q_{ff} and Q_{fb} are front and back fixed interface charges, respectively. The terminal charging/discharging currents are characterized using the quasi-static approximation:

$$\frac{dQ_i}{dt}=\sum_j \frac{\partial Q_i}{\partial V_j}\frac{dV_j}{dt} \quad (26)$$

where $i = S, D, Gf, Gb, B$ and $j = DS, GfS, GbS, BS$. Note that (26) defines nonreciprocal capacitances and transcapacitances that physically reflect the charge dynamics of the five-terminal device.

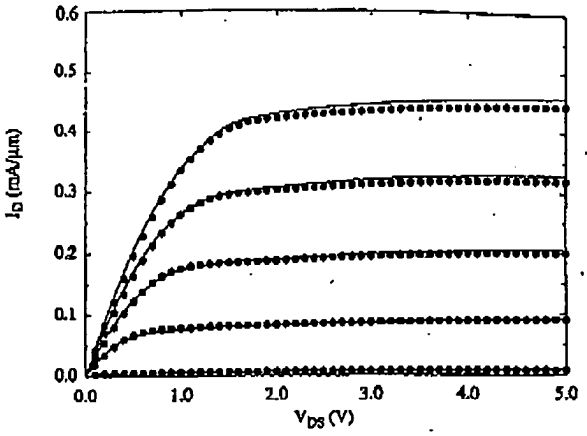

Fig. 4. Model- (curves) and MEDICI-predicted $I_D - V_{DS}$ characteristics for an $L = 0.5$ μm n-channel NFD/SOI MOSFET; $V_{GfS} = 15$ V, $V_{BS} = 0$.

III. Verification/Demonstration

We implemented the new model in SOISPICE [7], expanding it for use in NFD/SOI as well as FD/SOI CMOS technologies. The network representation of the implemented model is shown in Fig. 3. The lumped resistances R_{LDS} and R_{LDD} account for the ohmic voltage drops in the LDD/LDS regions, if these regions are part of the device structure. The element V_{LDD} represents the non-ohmic portion of the LDD voltage drop. Since it depends on the channel analysis, it necessitates an iterative Newton-like solution in the model algorithm as noted in Section II. The body node is optional. When it is not specified on the device line, the model formalism floats the body and implicitly accounts for all floating-body effects. Underlying this accounting is nonzero V_{BS}, which is implied by the nodal equation $I_R = I_{Gi} + I_{Gt}$ in dc simulations but is influenced by dQ_B/dt is transient simulations as indicated in Fig. 3.

To get preliminary support for the model and to confirm its predictive capabilities, we compared results of SOISPICE device simulations with those of MEDICI [16], a numerical two-dimensional device simulator. In contrast to empirical SPICE models, our NFD/SOI MOSFET model is physical and its parameters are structure-dependent, including, for example, oxide thicknesses and regional dimensions and doping densities indicated in Fig. 1. The parameters thus can be effectively defined from the device structure and physical models, e.g., mobility versus doping, used by MEDICI; no rigorous parameter extraction/optimization is needed. For example, t_b was the actual depth of the (abrupt) high–low junction specified for the MEDICI simulations. A wide variety of device structures, with channel lengths ranging down to 0.2 μm, were simulated successfully. The SOISPICE- and MEDICI-predicted current-voltage characteristics plotted in Figs. 4 and 5, for n-channel devices with the body terminal shorted to the source terminal, exemplify the model verification and demonstration. The predicted $I_D - V_{DS}$ characteristics for an $L = 0.5$ μm device in Fig. 4 are in good agreement for all V_{GfS} above threshold. The predicted subthreshold $I_D - V_{GfS}$ characteristics in Fig. 5 for varying gate oxide thickness (t_{of}) and effective film thickness

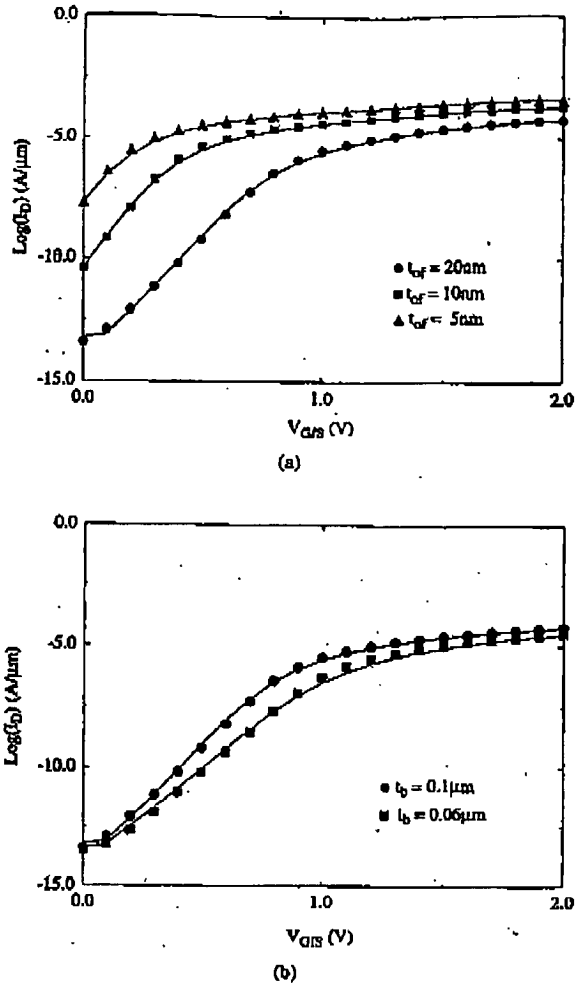

Fig. 5. Model- (curves) and MEDICI-predicted subthreshold $I_D - V_{GfS}$ characteristics for an $L = 0.8$-μm n-channel NFD/SOI MOSFET for varying (a) t_{of} and (b) t_b; $V_{DS} = 0.1$ V, $V_{BS} = 0$.

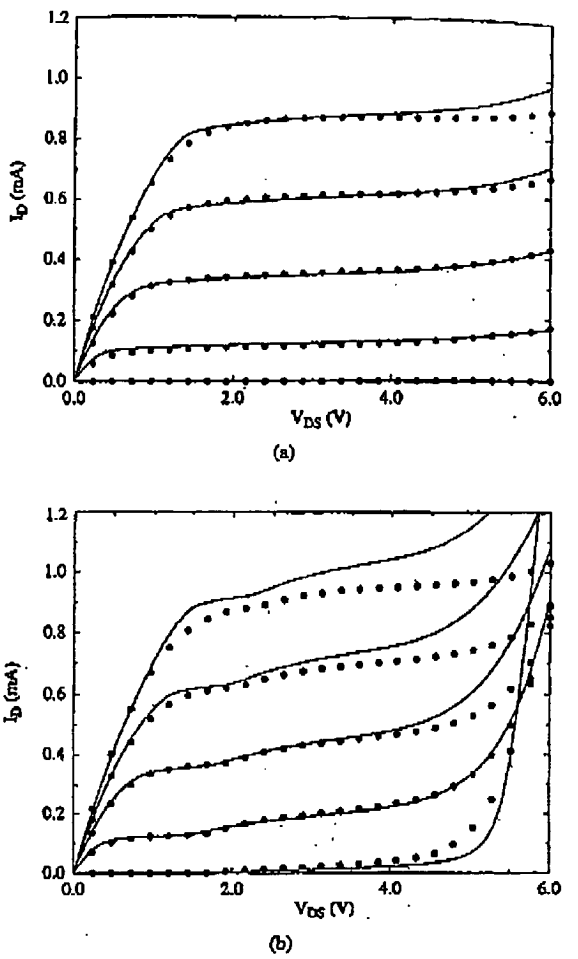

Fig. 6. Measured (points) and model-predicted $I_D - V_{DS}$ characteristics for a $W/L = 2.4$-μm/0.6-μm n-channel NFD/SOI MOSFET with LDD/LDS and halo, with (a) body tied and (b) body floating; $V_{GfS} = 1$–5 V.

(t_b) in an $L = 0.8 - \mu$m device show excellent agreement as well.

For additional verification, we compared model predictions with measured data taken from test devices of two different NFD/SOI technologies, each having a wide range of channel lengths. Again the model parameters were determined in large part using device structural information, but some minor tuning was done because the available information was incomplete. For example, t_b was tuned, based on (16) and (17), to be in accord with the measured subthreshold slope at low V_{DS}. The values thereby derived were nearly equal to the calculated maximum depletion widths for the doping profiles provided, which is consistent with the model assumptions.

In the first technology, the devices were fabricated on SIMOX wafers having a 400-nm buried oxide and a 300-nm silicon film, with LDD/LDS and halo implants. The gate oxide is 20-nm thick, and the gate is n^+ polysilicon. The devices have external body contacts, so both floating-body and body-tied (to source) characteristics could be measured. Results of the model application to this technology are exemplified in Fig. 6 where measured and predicted $I_D - V_{DS}$ characteristics of an n-channel device with an effective channel length of 0.6 μm are plotted. The SOISPICE predictions for both tied-body and floating-body cases, done with a single set of model parameters, are generally good. The discernible floating-body effects, i.e., the premature breakdown, the saturation-current kink, and a low-V_{DS} current enhancement, are modeled well. The latter effect has not been acknowledged well in previous work, but it is indeed significant. For example, at $V_{GfS} = 2$ V and V_{DS} less than the kink onset voltage, the enhancement is approximately 20%; it is higher for lower V_{GfS}. Note that there is evidence of premature breakdown even in the tied-body characteristics; this is due to the finite body resistance in the body-source tie, which supports a nonzero V_{BS} when impact-ionization current is injected into the body [17].

In the second technology, the devices were more aggressively scaled. They were fabricated on SOI substrates having 360-nm buried oxide and 75-nm silicon film, without LDD/LDS or halo. The gate oxide thickness is 5 nm, and there is no body tie. The model application to this technology is exemplified by the measured and simulated current–voltage characteristics in Fig. 7 for a floating-body n-channel device

with an effective channel length of 0.2 μm. The $I_D - V_{DS}$ characteristics in Fig. 7(a) show good agreement, although some discrepancy is obvious at high I_D and V_{DS}, as it is in Fig. 6 to a lesser extent. These discrepancies are attributed to self-heating in the SOI MOSFET under dc bias producing substantive power dissipation [18], which is not accounted for in the model. As implied by the figures, the primary effect of self-heating in these devices is an amelioration of impact ionization: the current kink is reduced and the breakdown voltage is increased. The same floating-body effects noted in Fig. 6(b) are obvious in Fig. 7(a). The subthreshold $I_D - V_{GfS}$ characteristics in Fig. 7(b), which also show very good agreement, however, reveal another floating-body effect at high V_{DS}: the increased slope (supra-ideal $S = 44$ mV) reflects a subthreshold kink.

IV. Floating-Body Effects

The dc floating-body effects revealed in Figs. 6 and 7 (premature breakdown, saturation-region and subthreshold kinks, and low-V_{DS} current enhancement) are modeled well by SOISPICE, which can thus give physical insight regarding their origin in the NFD device. All of the effects are due to excess majority-carrier charge in the body, injected via carrier generation, which can be removed only via recombination. Finite carrier lifetimes thus define a forward bias V_{BS} on the body–source junction, which drives the mentioned effects. The premature breakdown [14], which is equivalent to the off-state latch [15], results when V_{BS} activates the parasitic BJT and when V_{DS} is high enough that the BJT current produces significant impact ionization, which in turn injects more charge in the body and causes the process to become regenerative. The other effects are due to the sensitivity of the NFD threshold voltage to V_{BS} (which is negligible in the FD device). The kink effects are driven by impact ionization as well, but at values of V_{DS} too low to cause regeneration. In strong inversion, the kink in saturation current results as V_{BS} reaches a "diode drop" [15]; in weak inversion, the kink is reflected as an abnormally high slope, or low gate voltage swing S, defined by the increasing V_{BS} [19] and not necessarily correlated with the activation of the parasitic BJT. The low-V_{DS} current enhancement, which occurs prior to the kink, is not well known. It is driven by thermal carrier generation. In addition to these dc floating-body effects, transient body charging can cause a current overshoot [20] defined by $V_{BS}(t) > 0$ and an "undershoot" defined by $V_{BS}(t) < 0$, both of which reflect dynamic threshold voltages.

In a viable NFD/SOI CMOS technology, all of the floating-body effects must be recognized, and either inhibited or exploited pragmatically. Obviously the BJT-induced breakdown is detrimental and must be controlled; the potential benefit afforded by the supplemental BJT current drive in digital applications is small and is preempted by the associated loss of gate control [7]. However, the effects due to V_{BS}-defined threshold voltage could possibly be exploited pragmatically to benefit performance. The reliable device/circuit simulation capability afforded by SOISPICE with our NFD/SOI MOSFET model can be used to check this exploitation of the floating-body effects.

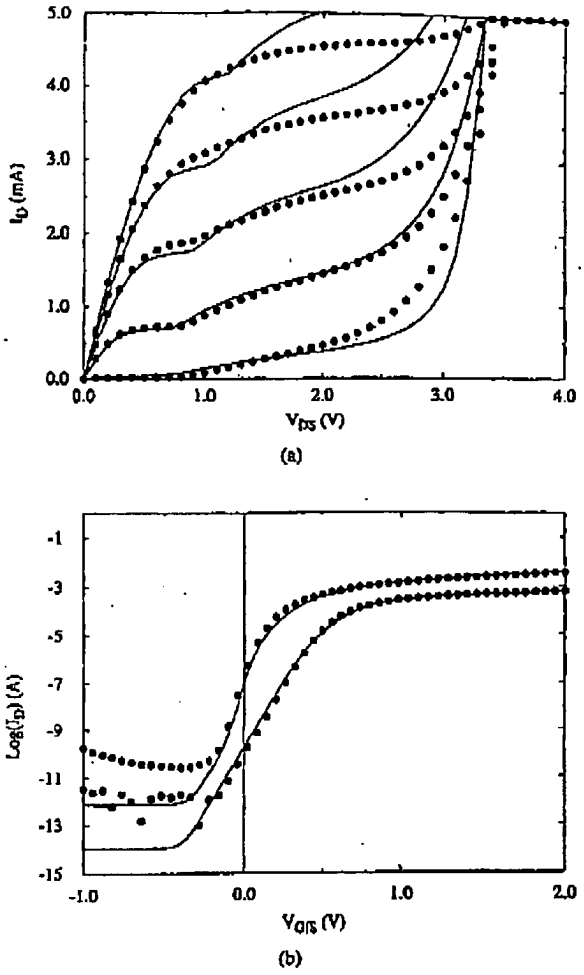

Fig. 7. Measured (points) and model-predicted (a) $I_D - V_{DS}$ and (b) $I_D - V_{GfS}$ characteristics for a $W/L = 10$-μm/0.2-μm n-channel NFD/SOI MOSFET with floating body. In (a) $V_{GfS} = 0.5$–2.5 V; in (b) $V_{DS} = 0.1$, 2.0 V.

Exploitation of the kink effects is risky since they are driven by impact ionization, which also drives the parasitic BJT and the ultimate loss of gate control. It is obvious from Figs. 6(b) and 7(a) that attempting to design for a supply voltage above the saturation-current kink but below breakdown is nonsensical. However, it is not so obvious that designing to exploit the subthreshold kink (Fig. 7(b)) is impractical. Very low S, much lower than the ideal 60 mV, is possible [19]. If such a low S could be achieved in a viable design, then possibly the threshold voltage could be reduced to get higher current drive and faster speeds, without threatening off-state ($V_{GfS} = 0$) current and standby-power restrictions [6].

Insight from our model suggests that $S < 60$ mV can be achieved by controlling the $I_R(V_{BS})$ dependence in (23). From (16) and (17), we can approximate the gate voltage swing as

$$S = \left(\frac{d \log I_D}{dV_{GfS}}\right)^{-1} \cong \frac{S_0}{\left(1 + \alpha \frac{\partial V_{BS}}{V_{GfS}}\right)} \qquad (27)$$

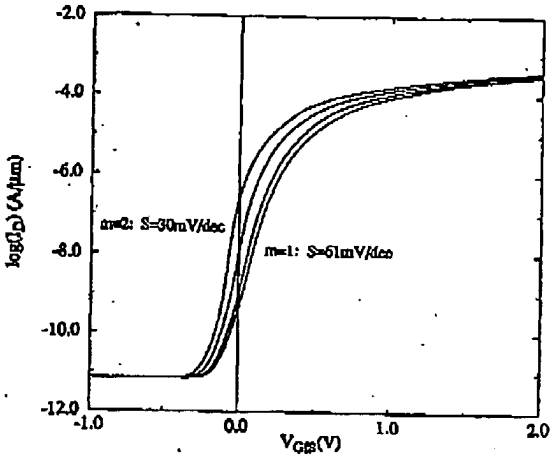

Fig. 8. Model-predicted subthreshold $I_D - V_{GfS}$ characteristics for varying m; $L = 0.2$ μm, $V_{DS} = 2$ V.

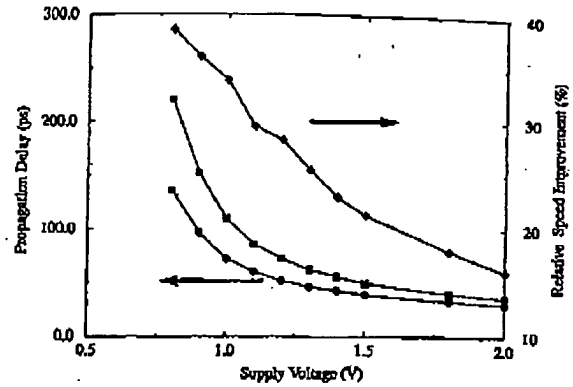

Fig. 9. SOISPICE-predicted gate propagation delays versus supply voltage for floating (•) and tied (■) bodies; $L = 0.2$ μm. The delays were derived from unloaded three-stage NFD/SOI CMOS inverter-chain simulations. Also shown is the predicted relative speed improvement (♦) afforded by the floating body.

where $S_0 = V_{TH}(1+\alpha)\ln(10)$, which is the normal value of S when $V_{BS} = 0$. (Note that $\alpha > 0$ defines $S_0 > 60$ mV for the NFD/SOI MOSFET.) The reduction of S in the floating-body device (at high V_{DS}) is characterized by the derivative in the denominator of (27), which is defined by I_R and the impact-ionization current I_{Gi} in this case. Since $I_R \cong I_{Gi} \cong (M-1)I_{CH}$, (27) with (23) yields

$$S \cong S_0 - m\alpha V_{TH}\, ln\,(10). \tag{28}$$

Note from (28) that when the nonideality factor m for I_R is unity, $S = V_{TH}\ln(10) = 60$ mV. Thus only when $m > 1$ can S be less than the ideal value. Such is the case in typical NFD/SOI MOSFET's as evidenced in Fig. 7(b). In essence, a higher m defines a higher V_{BS} for a given I_{Gi}, and hence a more significant subthreshold kink. This dependence on m is illustrated in Fig. 8 where SOISPICE-simulated subthreshold characteristics for varying m are shown. Note that for $m = 2$, a physical upper limit, S is extremely low, but the off-state current is very high.

The high off-state current is a problem, but does the abnormally low S actually imply a speed benefit? No, according to SOISPICE circuit simulations. Predicted propagation delays taken from simulations of CMOS inverter chains using different values of m in the I_R model, compared with delays predicted when the impact ionization was turned off, show that the subthreshold kink, irrespective of m as well as the load and the supply voltage V_{DD}, yields no speed improvement. This result is attributed to the dynamic nature of the inverter circuit. The added drive current afforded by the kink, that is, by the I_{Gi}-driven threshold reduction, is significant only for high V_{DS} and low V_{GfS}. For V_{DD} larger than the kink onset voltage, these voltage conditions are not simultaneously prevalent during most of the switching time; for lower V_{DD}, there is no kink effect. We conclude then that the kink is not beneficial, and in fact is detrimental with regard to off-state current as evidenced in Fig. 8. It must be suppressed, which is compatible with inhibiting the BJT-induced loss of gate control.

The low-V_{DS} current enhancement evident as a floating-body effect in Fig. 6 is driven by thermal generation current (I_{Gt}). For dc conditions at low V_{DS} (where impact ionization is negligible), $I_R = I_{Gt}$ defines

$$V_{BS} = mV_T \ln\left(1 + \frac{I_{Gt}}{WJ_{R0}}\right). \tag{29}$$

Depending on the ratio I_{Gt}/WJ_{R0}, this body bias can reduce the device threshold voltage and thereby enhance current. Typically, as reflected by Fig. 6 and quantified by additional SOISPICE simulations with floating and tied bodies, V_{BS} in (29) can be a few tenths of a volt and can produce a significant enhancement in saturation current. For example, for the $L = 0.2$ μm device of Fig. 7, the predicted current enhancement is about 50% at $V_{GfS} = V_{DS} = 1.0$ V and about 20% at $V_{GfS} = V_{DS} = 2.0$ V, suggesting exploitation of this effect for low-voltage CMOS applications. Note that the enhancement could be partly due to an intrinsic $V_{BS} < 0$ in the tied-body device, which increases the threshold voltage, because of internal ohmic drops in the source region. Nonetheless, the advantage of the floating body in this regard is palpable.

In transient operation of the device, this current enhancement will tend to prevail; a "latent" $V_{BS} > 0$, driven predominantly by I_{Gt} as described in (29) when the device is turned on, will be sustained for all finite V_{DS}, even though the body charging current (dQ_B/dt in Fig. 3) will tend to modulate it. This insight is confirmed by the SOISPICE-predicted gate propagation delays plotted in Fig. 9 versus supply voltage (V_{DD}). The delays were derived from simulations of unloaded three-stage CMOS inverter-chain circuits using NFD/SOI devices represented in Fig. 7, in both floating- and tied-body configurations. A significant speed improvement due to the latent V_{BS} in the floating-body device is predicted. As V_{DD} is scaled down, the delay increases due to smaller current drive, but the relative magnitude of the speed benefit due to the latent V_{BS} increases. Thus this particular floating-body effect is advantageous for low-voltage CMOS applications, and its benefit will be more pronounced the lower V_{DD} is and the higher the (capacitive) loads are.

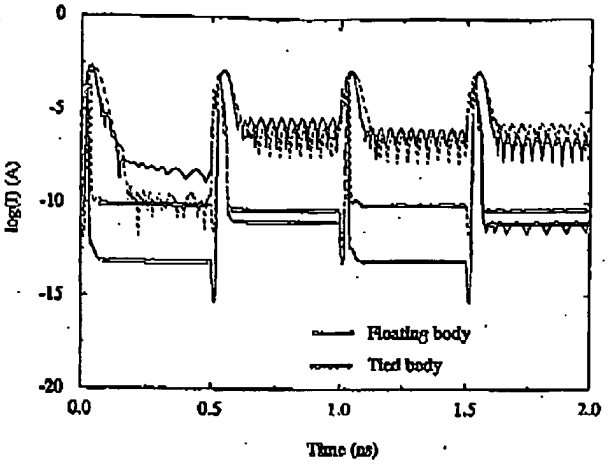

Fig. 10. SOISPICE-predicted transient currents in the middle stage of the three-stage NFD/SOI CMOS inverter chain, with floating and tied bodies; $L = 0.2\ \mu$m, $V_{DD} = 1.5$ V. The physical off-state leakage (channel) currents are highlighted; the noisy currents reflect errors associated with the integration method used in SPICE.

However, this speed improvement would seem to imply a common design tradeoff because it results from effective threshold lowering which would also increase off-state current and hence static power. Fortunately, the transient circuit simulations suggest though that this tradeoff is not needed; they show that the benefit is not undermined by increased off-state current because of a unique dynamic floating-body effect in the NFD/SOI MOSFET. As indicated by the SOISPICE-predicted transient currents in the CMOS inverter chain, plotted in Fig. 10 for floating and tied bodies, the dynamic off-state current is effectively suppressed when the body is floating. The suppression occurs because the MOSFET body is partially depleted of majority carriers in the on state, and the depletion charge in the off state forces $V_{BS}(t) < 0$ as the carriers are recovered. Whereas the time constant associated with this recovery in the tied-body device (i.e., the dielectric relaxation time) is negligibly short and thus V_{BS} becomes zero almost instantaneously, that for the floating-body device (i.e., a carrier generation lifetime) is very long compared with operating periods of high-frequency signals in scaled CMOS circuits: the depletion charge can only be neutralized by the reverse saturation currents of the source/drain-body p-n junctions in the floating-body device. Thus $V_{BS} < 0$ is predominant during the off-state period of the floating-body device, and the current is suppressed because of the implied higher threshold. The static power in the circuit is effectively decreased by this current "undershoot."

The floating-body effect due to transient body charging [20] is the counterpart to the dynamic suppression of off-state current. As the MOSFET is switched from off to on, excess majority carriers are stored in the body until they recombine. The concomitant $V_{BS}(t) > 0$ lowers the threshold voltage, thereby producing a transient drain current overshoot. The magnitude of the overshoot depends on how efficiently the majority carriers are replenished in the off state by carrier generation. As noted above, this replenishment is typically not efficient, and hence the overshoot is usually negligible. SOISPICE simulations of CMOS inverter circuits, using representative carrier lifetimes to define I_R in (23) and I_{Gt} in (24), confirm this and predict no significant reduction in propagation delay due to the overshoot.

We caution that dynamic floating-body benefits are hysteretic; every cycle depends on the history of device dynamics as indicated by the difference between the off-state currents in Fig. 10 for the floating-body circuit. Hence pragmatic exploitation of the beneficial dynamic effects will necessitate circuit as well as device design scrutiny and innovation. Furthermore, the SOI device self-heating effects [18] in dynamic circuit operation will have to be recognized.

V. Summary

A physical charge-based model for the NFD/SOI MOSFET has been presented. The model expands the TFA formalism in [8] to account for body doping variations and LDD/LDS regions and to characterize the channel current in weak- and moderate-inversion regions. It also includes the generation currents due to impact ionization and thermal generation, and the parasitic-BJT and recombination currents in the device, as well as charge modeling for dynamic simulation. The model is implemented in SOISPICE and verified by numerical device simulations as well as measured test-device data. The model predicts the various floating-body effects reliably since it physically characterizes the floating-body voltage (i.e., V_{BS}) both in dc and in transient operations. The floating-body effects in NFD/SOI CMOS were investigated using SOISPICE. The subthreshold slope can be less than 60 mV in the floating-body device depending on the nonideality of the source–body junction. Circuit simulations, however, reveal that this kink effect does not yield any speed enhancement, but is detrimental due to the higher off-state current. The "latent" body charging and $V_{BS} > 0$, driven by the thermal generation current, lower the threshold of the device and thus increase the current drive, improving CMOS speed. The implied increase in the off-state current is negated by a transient current undershoot due to $V_{BS}(t) < 0$, which is supported by charge dynamics. The beneficial dynamic floating-body effects, however, are hysteretic, and hence tend to produce circuit instabilities. Their pragmatic exploitation will require insightful device and circuit design, but could underlie significant advantages of SOI over bulk-silicon CMOS for low-voltage applications.

References

[1] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. Boston: Kluwer, 1991.
[2] J. G. Fossum and S. Krishnan, "Current-drive enhancement limited by carrier velocity saturation in deep-submicrometer fully depleted SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 40, p. 457, Feb. 1993.
[3] P. C. Yeh and J. G. Fossum, "Subthreshold MOSFET conduction model and optimal scaling for deep-submicron fully depleted SOI CMOS," in *Proc. IEEE Int. SOI Conf.*, Oct. 1993, p. 142.
[4] R. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: From bulk to SOI to bulk," *IEEE Trans. Electron Devices*, vol. 39, p. 1704, July 1992.
[5] C. F. Codella and S. Ogura, "Halo doping effects in submicron DI-LDD device design," in *IEDM Tech. Dig.*, p. 230, 1985.
[6] G. G. Shahidi, T. H. Ning, T. I. Chappell, J. H. Comfort, B. A. Chappell, R. Franch, C. J. Anderson, P. W. Cook, S. E. Schuster, M. G. Rosenfield, M. R. Polcari, R. H. Dennard, and B. Davari, "SOI for a 1-volt CMOS

technology and application to a 512 Kb SRAM with 3.5 ns access time," *IEDM Tech. Dig.*, p. 813, Dec. 1993.
[7] J. G. Fossum, P. C. Yeh, and J.-Y. Choi, "Computer-aided performance assessment of fully depleted SOI CMOS VLSI circuits," *IEEE Trans. Electron Devices*, vol. 40, p. 598, Mar. 1993.
[8] S. Veeraraghavan and J. G. Fossum, "A physical short-channel model for the thin-film SOI MOSFET applicable to device and circuit CAD," *IEEE Trans. Electron Devices*, vol. 35, p. 1866, Nov. 1988.
[9] R. L. Burden and J. D. Fairea, *Numerical Analysis*, 4th ed. Boston: PWS-Kent, 1989.
[10] Y. Tsividis, "Moderate inversion in MOS devices," *Solid-State Electron.*, vol. 25, p. 1099, 1982.
[11] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.
[12] H. K. Lim and J. G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-30, p. 1244, Oct. 1983.
[13] K. R. Green and J. G. Fossum, "A simple two-dimensional model for subthreshold channel-length modulation in short-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. 40, p. 1560, Aug. 1993.
[14] K. K. Young and J. A. Burns, "Avalanche-induced drain-source breakdown in silicon-on-insulator n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, p. 426, Apr. 1988.
[15] J. Y. Choi and J. G. Fossum, "Analysis and control of floating-body bipolar effects in fully depleted submicrometer SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 38, p. 1384, June 1991.
[16] TMA-MEDICI: Two-Dimensional Device Simulation Program, ver. 1, Technology Modeling Associates, Inc., Palo Alto, CA, 1992.
[17] D. Suh and J. G. Fossum, "The effect of body resistance on the breakdown characteristics of SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, p. 1063, June 1994.
[18] L. T. Su, J. E. Chung, D. A. Antoniadis, K. E. Goodson, and M. I. Flik, "Measurement and modeling of self-heating in SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, p. 69, Jan. 1994.
[19] J. G. Fossum, R. Sundaresan, and M. Matloubian, "Anomalous subthreshold current-voltage characteristics of p-channel SOI MOSFET's," *IEEE Electron Device Lett.*, vol. 8, p. 544, Nov. 1987.
[20] H. K. Lim and J. G. Fossum, "Transient drain current and propagation delay in SOI CMOS," *IEEE Trans. Electron Devices*, vol. ED-31, p. 1251, Sept. 1984.

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Dr. Fossum is a member of the Honorary Editorial Advisory Board of *Solid-State Electronics*; he was an Associate Editor for the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN from 1988 to 1991. In 1983 he was elected a Fellow of the IEEE for contributions to the theory and technology of silicon solar cells and transistors. In 1992 he and two of his students received the Best Paper Award at the IEEE International SOI Conference.

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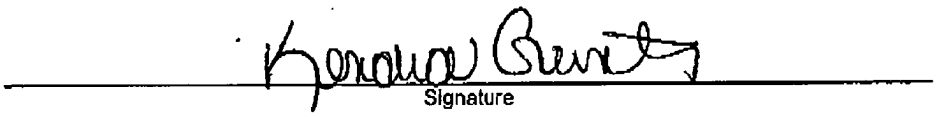
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